US009213783B2

(12) United States Patent
Hansen

(10) Patent No.: US 9,213,783 B2
(45) Date of Patent: Dec. 15, 2015

(54) **SOURCE MASK OPTIMIZATION TO REDUCE STOCHASTIC EFFECTS**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **13/719,135**

(22) Filed: **Dec. 18, 2012**

(65) **Prior Publication Data**

US 2013/0179847 A1 Jul. 11, 2013

Related U.S. Application Data

(60) Provisional application No. 61/585,136, filed on Jan. 10, 2012.

(51) **Int. Cl.**

G06F 17/50	(2006.01)
G03F 7/20	(2006.01)
G03F 1/70	(2012.01)

(52) **U.S. Cl.**

CPC ***G06F 17/50*** (2013.01); ***G03F 1/70*** (2013.01); ***G03F 7/70125*** (2013.01); ***G03F 7/70433*** (2013.01); ***G03F 7/70441*** (2013.01)

(58) **Field of Classification Search**

USPC 716/54

See application file for complete search history.

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Primary Examiner — Eric Lee

(74) *Attorney, Agent, or Firm* — Pillsbury Winthrop Shaw Pittman LLP

(57) **ABSTRACT**

Disclosed herein is a computer-implemented method for improving a lithographic process for imaging a portion of a design layout onto a substrate using a lithographic projection apparatus, the method comprising defining a multi-variable cost function, the multi-variable cost function being a function of a stochastic effect of the lithographic process.

27 Claims, 15 Drawing Sheets

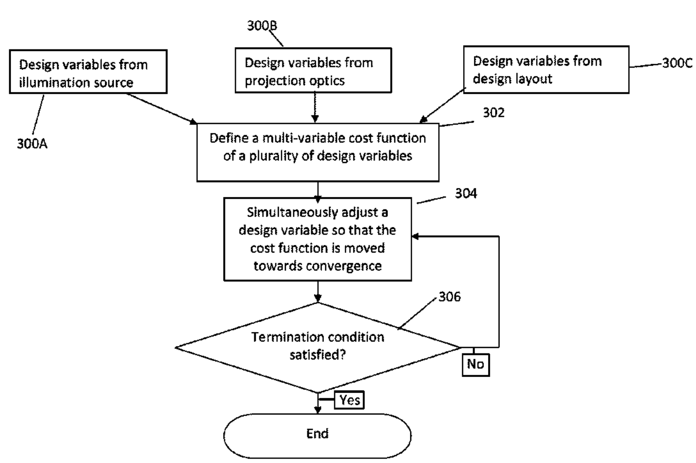

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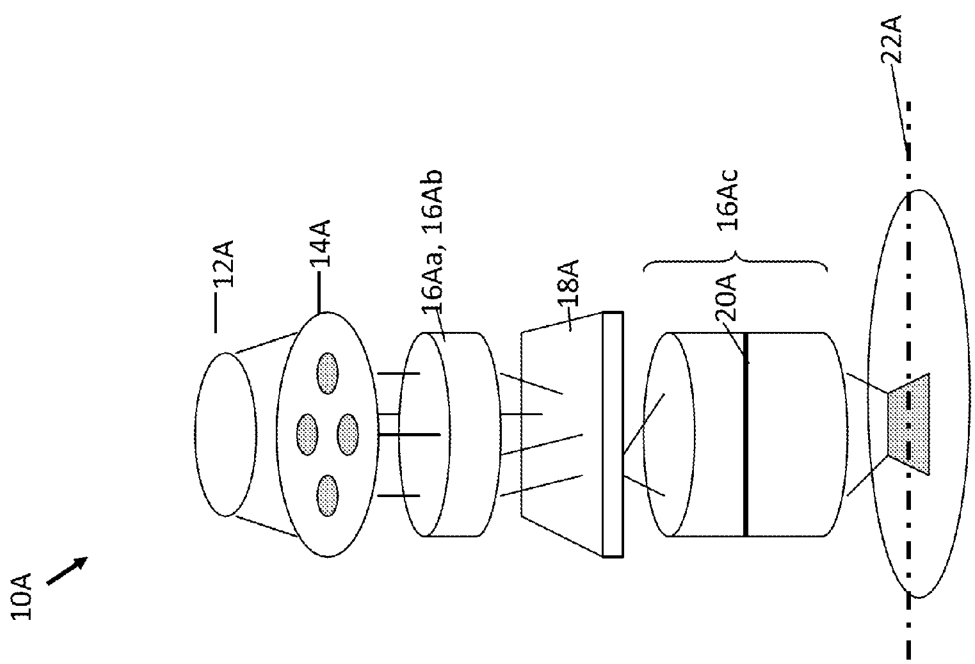
Fig. 1



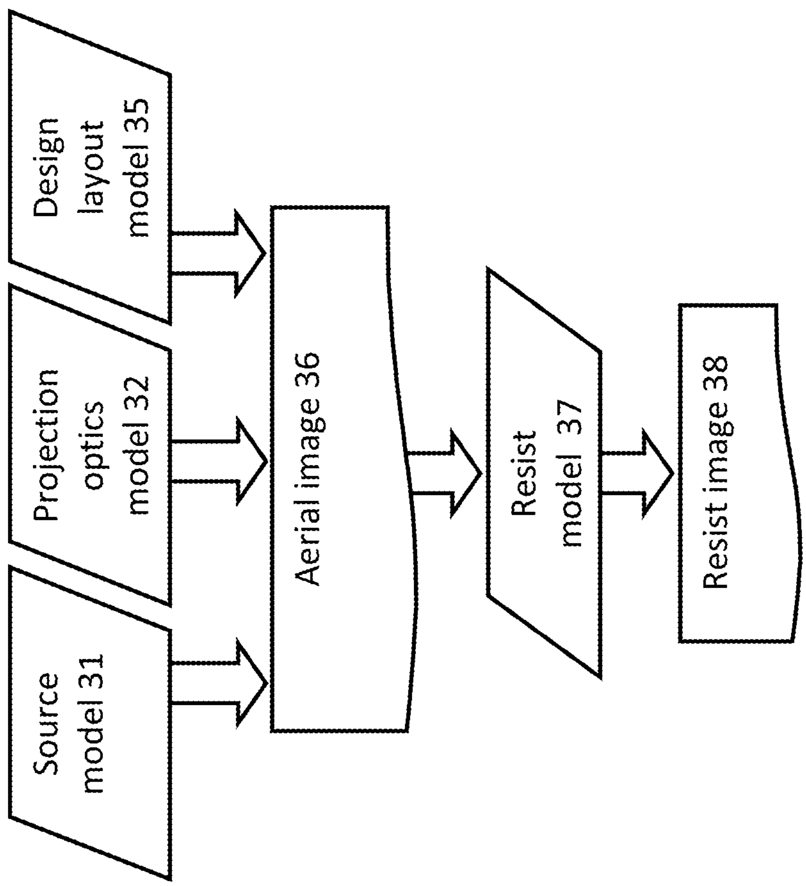

Design layout model 35
Projection optics model 32
Source model 31
Aerial image 36
Resist model 37
Resist image 38

Fig. 2

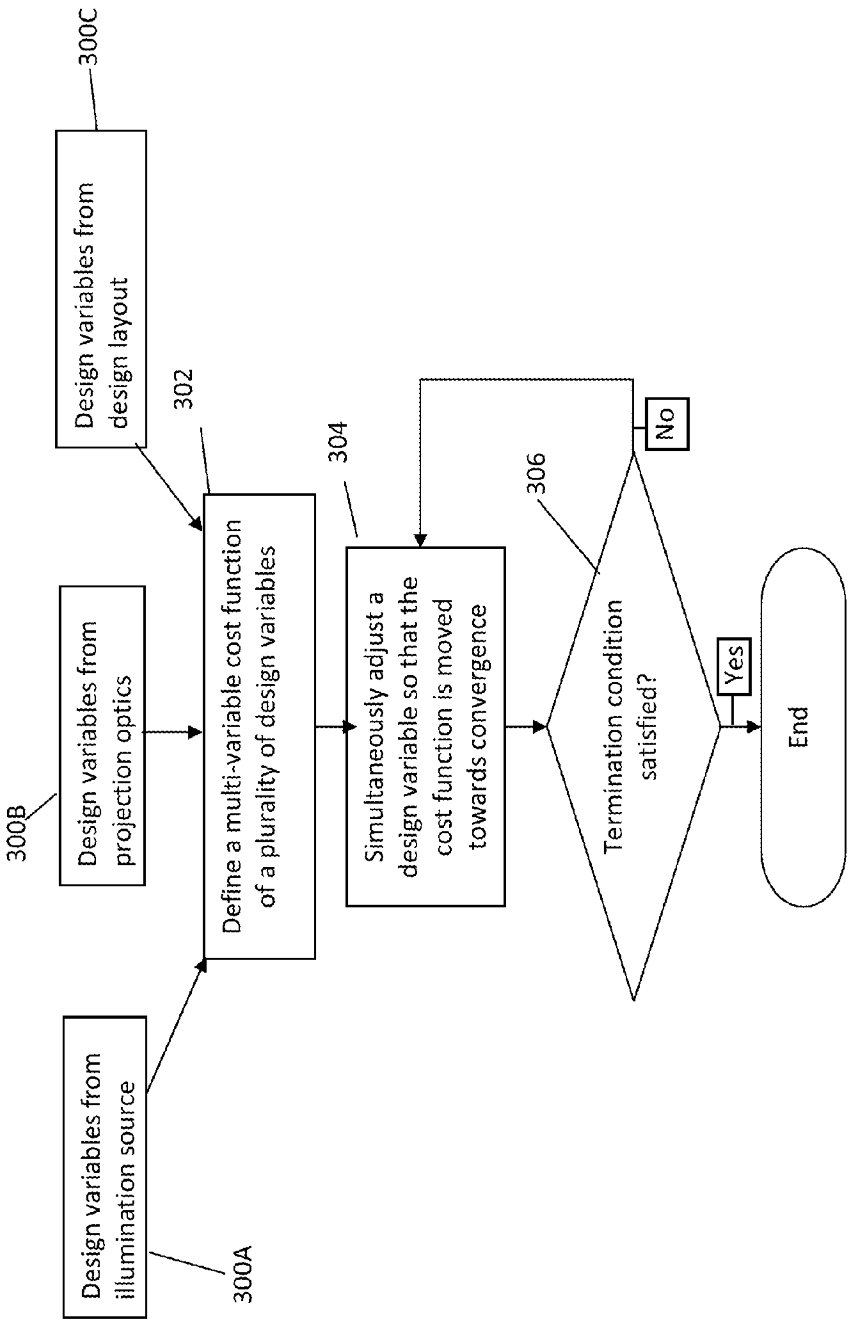

Design variables from illumination source
300A
Design variables from projection optics
300B
Design variables from design layout
300C
302
Define a multi-variable cost function of a plurality of design variables
304
Simultaneously adjust a design variable so that the cost function is moved towards convergence
306
Termination condition satisfied?
No
Yes
End

Fig. 3

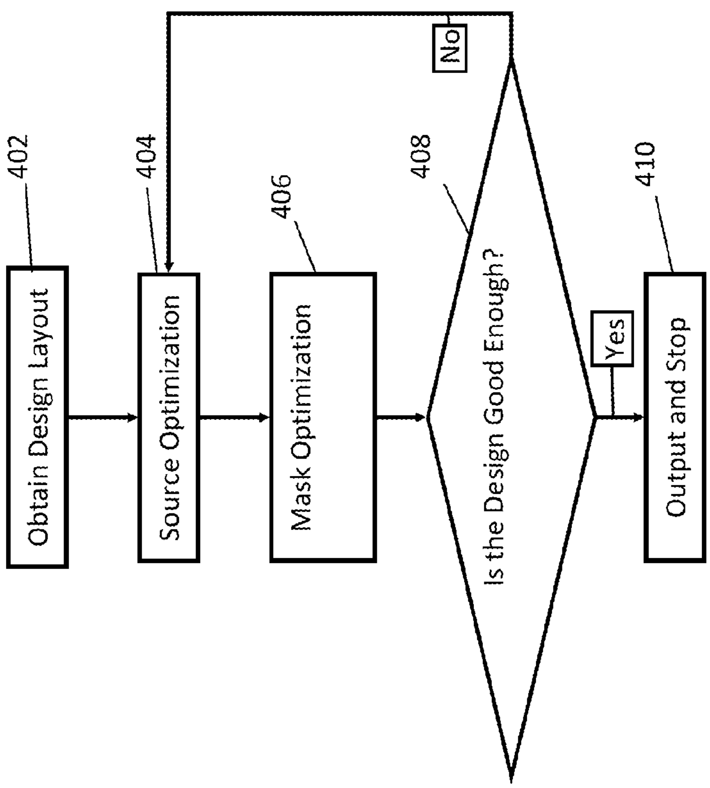

402
Obtain Design Layout
404
Source Optimization
406
Mask Optimization
408
Is the Design Good Enough?
No
Yes
410
Output and Stop

Fig. 4

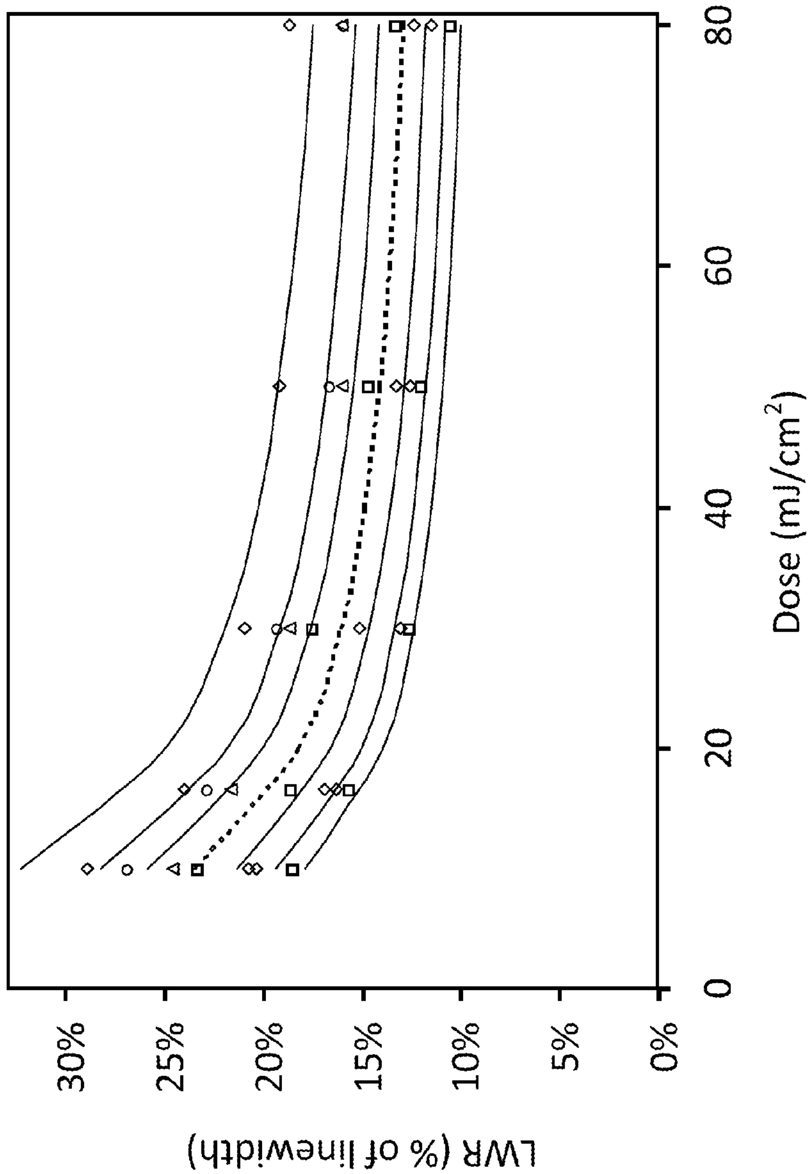


Fig. 5

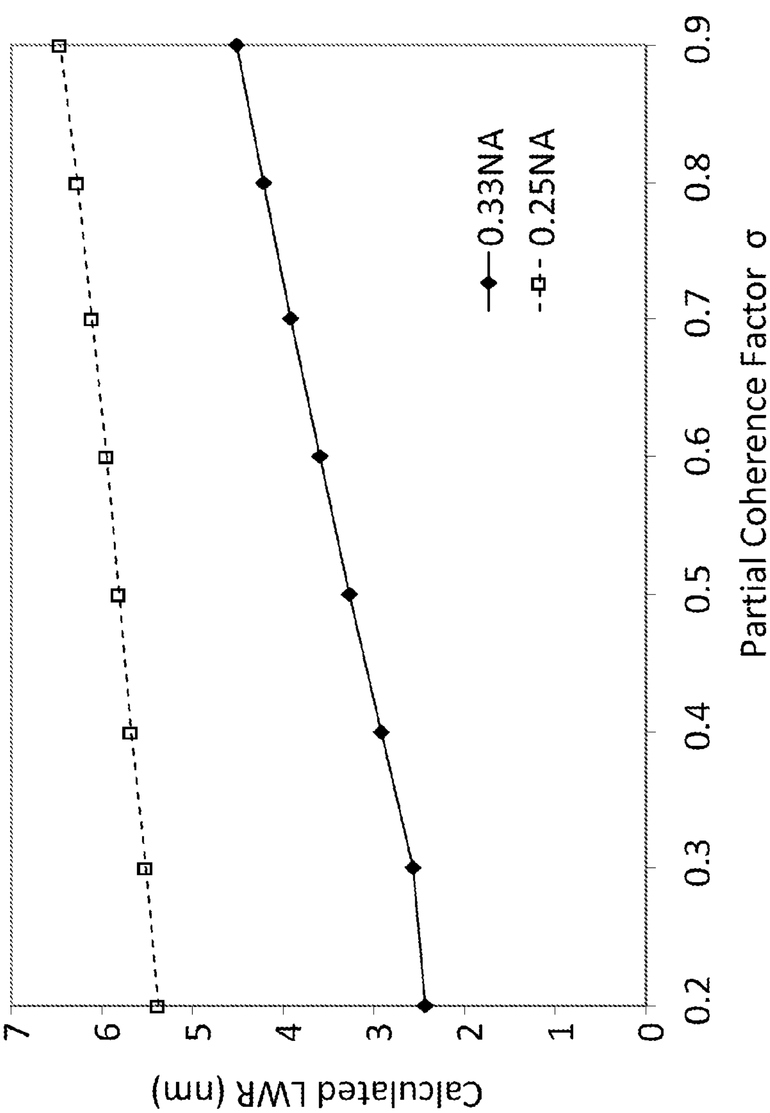

Calculated LWR (nm)
0
1
2
3
4
5
6
7
Partial Coherence Factor σ
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
0.33NA
0.25NA

Fig. 6

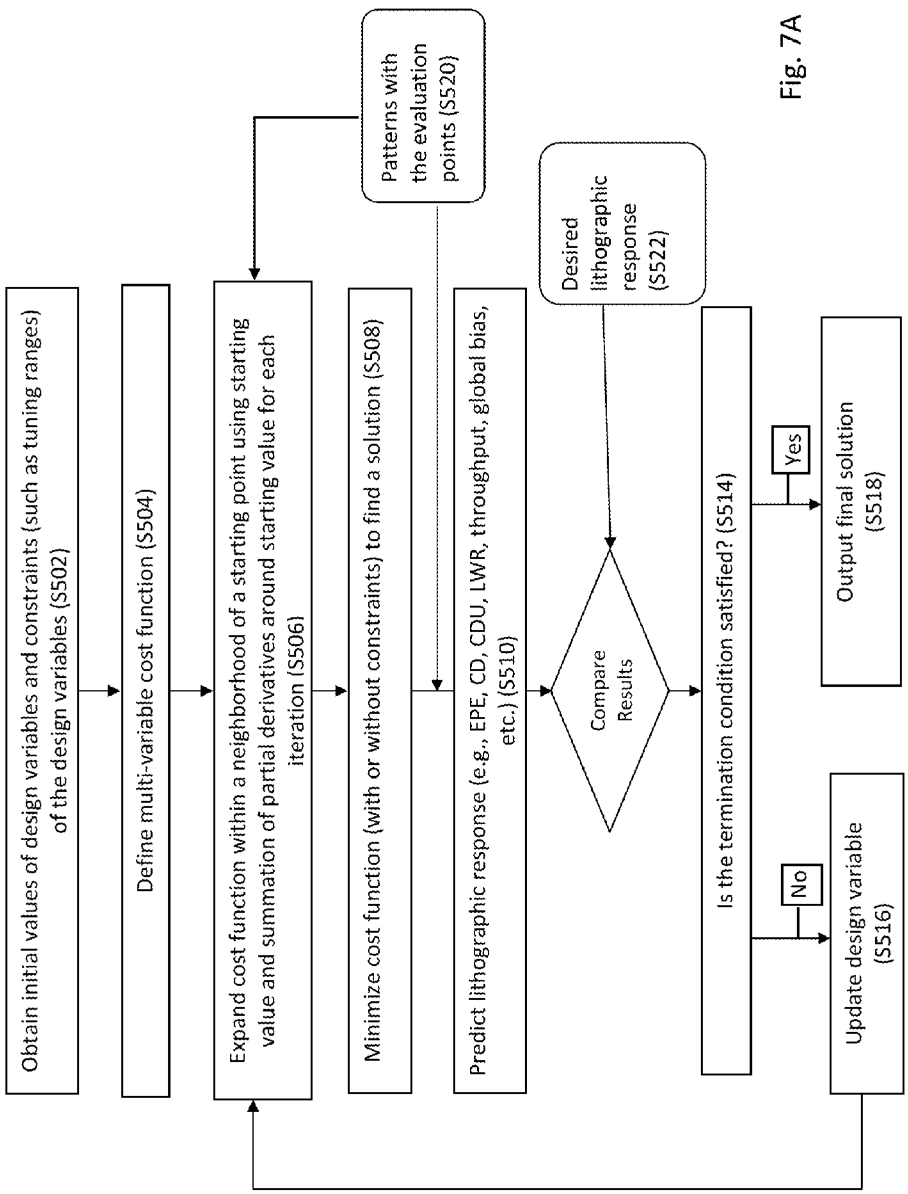

Obtain initial values of design variables and constraints (such as tuning ranges) of the design variables (S502)
Define multi-variable cost function (S504)
Expand cost function within a neighborhood of a starting point using starting value and summation of partial derivatives around starting value for each iteration (S506)
Patterns with the evaluation points (S520)
Minimize cost function (with or without constraints) to find a solution (S508)
Predict lithographic response (e.g., EPE, CD, CDU, LWR, throughput, global bias, etc.) (S510)
Desired lithographic response (S522)
Compare Results
Is the termination condition satisfied? (S514)
Yes
Output final solution (S518)
No
Update design variable (S516)

Fig. 7A

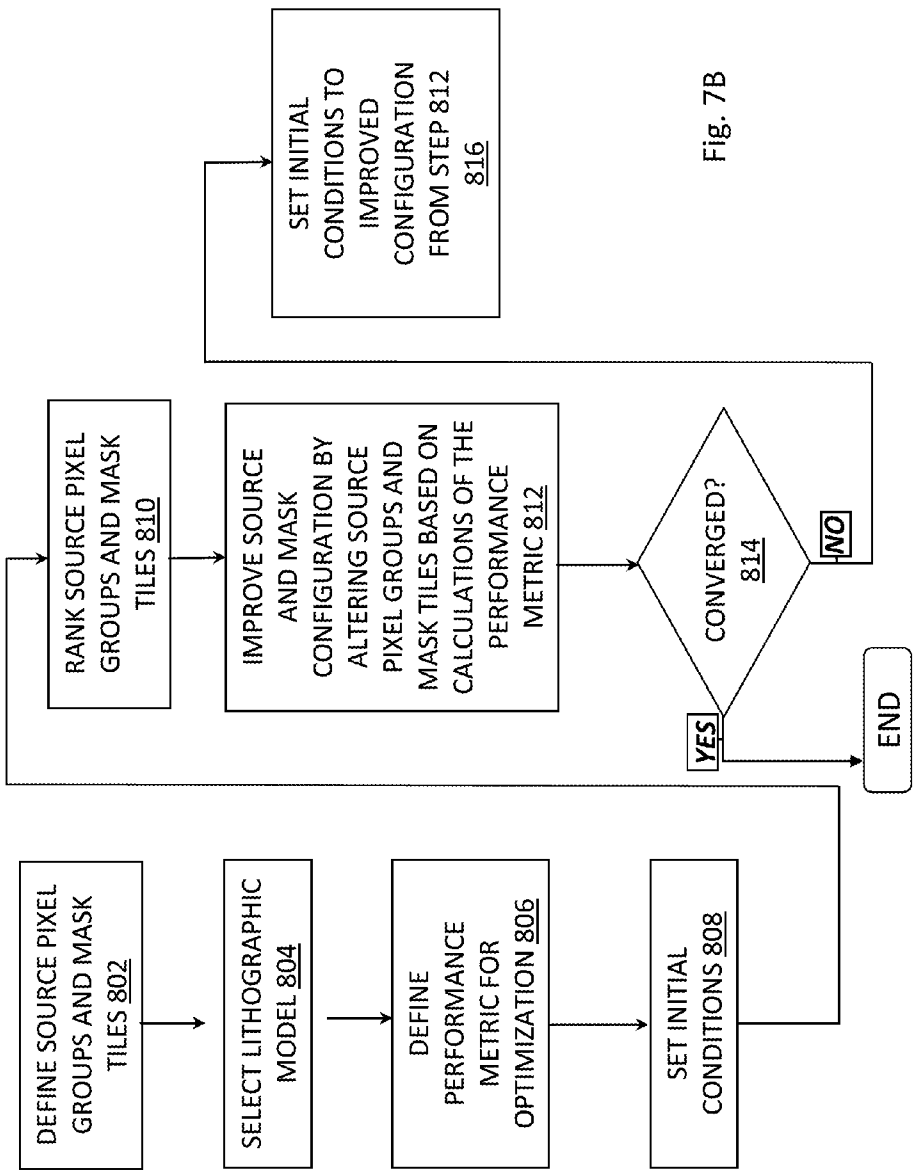

DEFINE SOURCE PIXEL GROUPS AND MASK TILES 802
SELECT LITHOGRAPHIC MODEL 804
DEFINE PERFORMANCE METRIC FOR OPTIMIZATION 806
SET INITIAL CONDITIONS 808
RANK SOURCE PIXEL GROUPS AND MASK TILES 810
IMPROVE SOURCE AND MASK CONFIGURATION BY ALTERING SOURCE PIXEL GROUPS AND MASK TILES BASED ON CALCULATIONS OF THE PERFORMANCE METRIC 812
CONVERGED? 814
NO
YES
SET INITIAL CONDITIONS TO IMPROVED CONFIGURATION FROM STEP 812 816
END

Fig. 7B

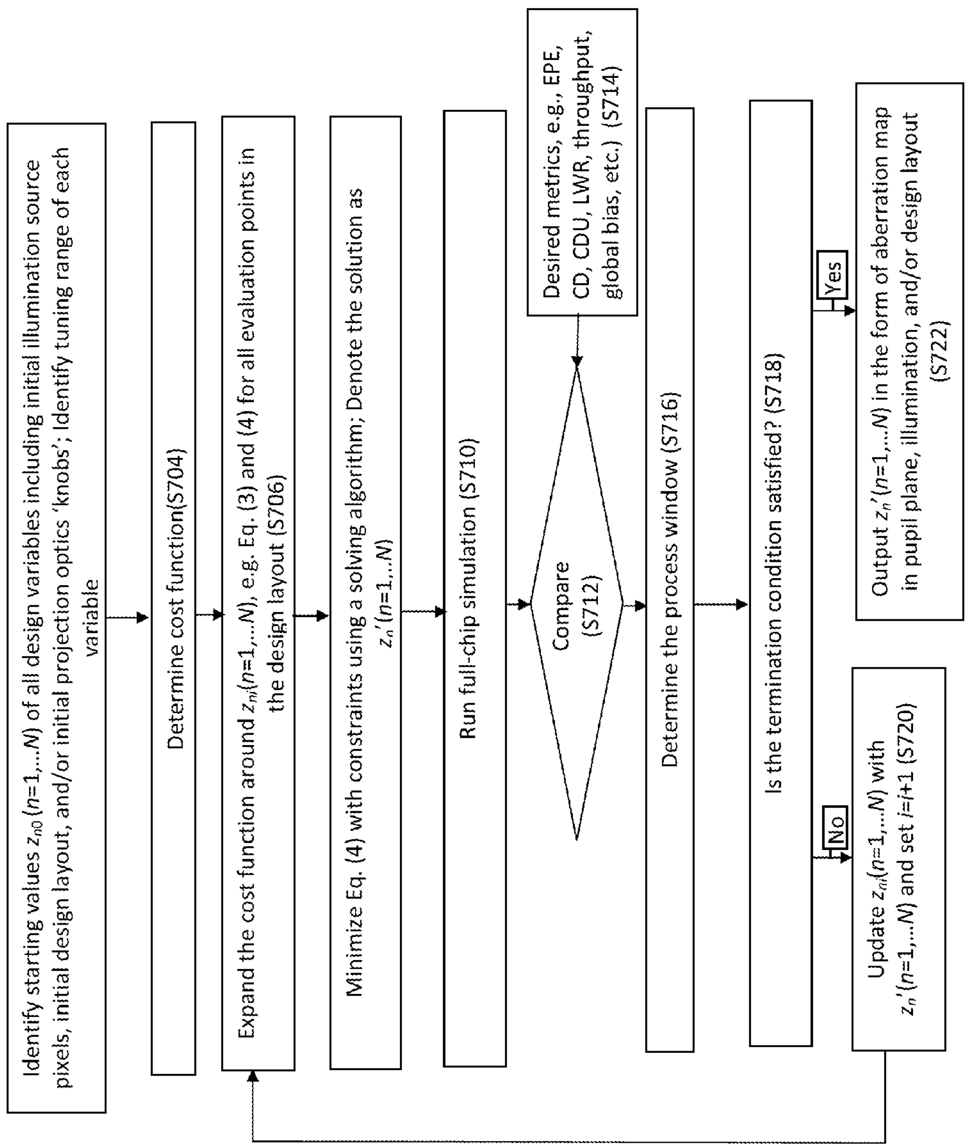

Identify starting values z_{n0} (n=1,...N) of all design variables including initial illumination source pixels, initial design layout, and/or initial projection optics 'knobs'; Identify tuning range of each variable
Determine cost function(S704)
Expand the cost function around z_{ni}(n=1,...N), e.g. Eq. (3) and (4) for all evaluation points in the design layout (S706)
Minimize Eq. (4) with constraints using a solving algorithm; Denote the solution as z_n'(n=1,...N)
Run full-chip simulation (S710)
Desired metrics, e.g., EPE, CD, CDU, LWR, throughput, global bias, etc.) (S714)
Compare (S712)
Determine the process window (S716)
Is the termination condition satisfied? (S718)
Yes
No
Output z_n'(n=1,...N) in the form of aberration map in pupil plane, illumination, and/or design layout (S722)
Update z_{ni}(n=1,...N) with z_n'(n=1,...N) and set i=i+1 (S720)

Fig.8

Eq. 7	CDU	Eq. 8
4.90 nm	2.46 nm	7.36 nm
2.52 nm	1.74 nm	4.26 nm

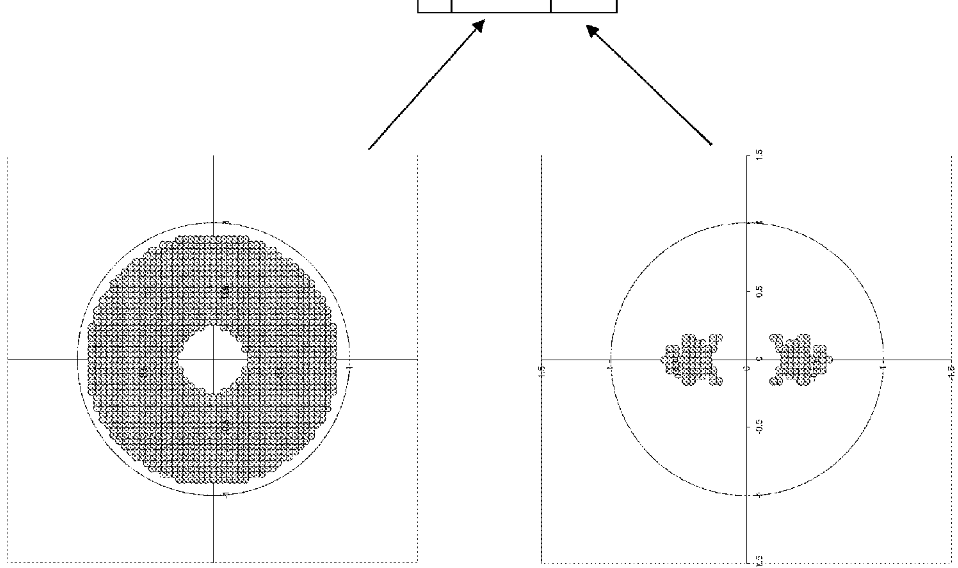


Fig. 9

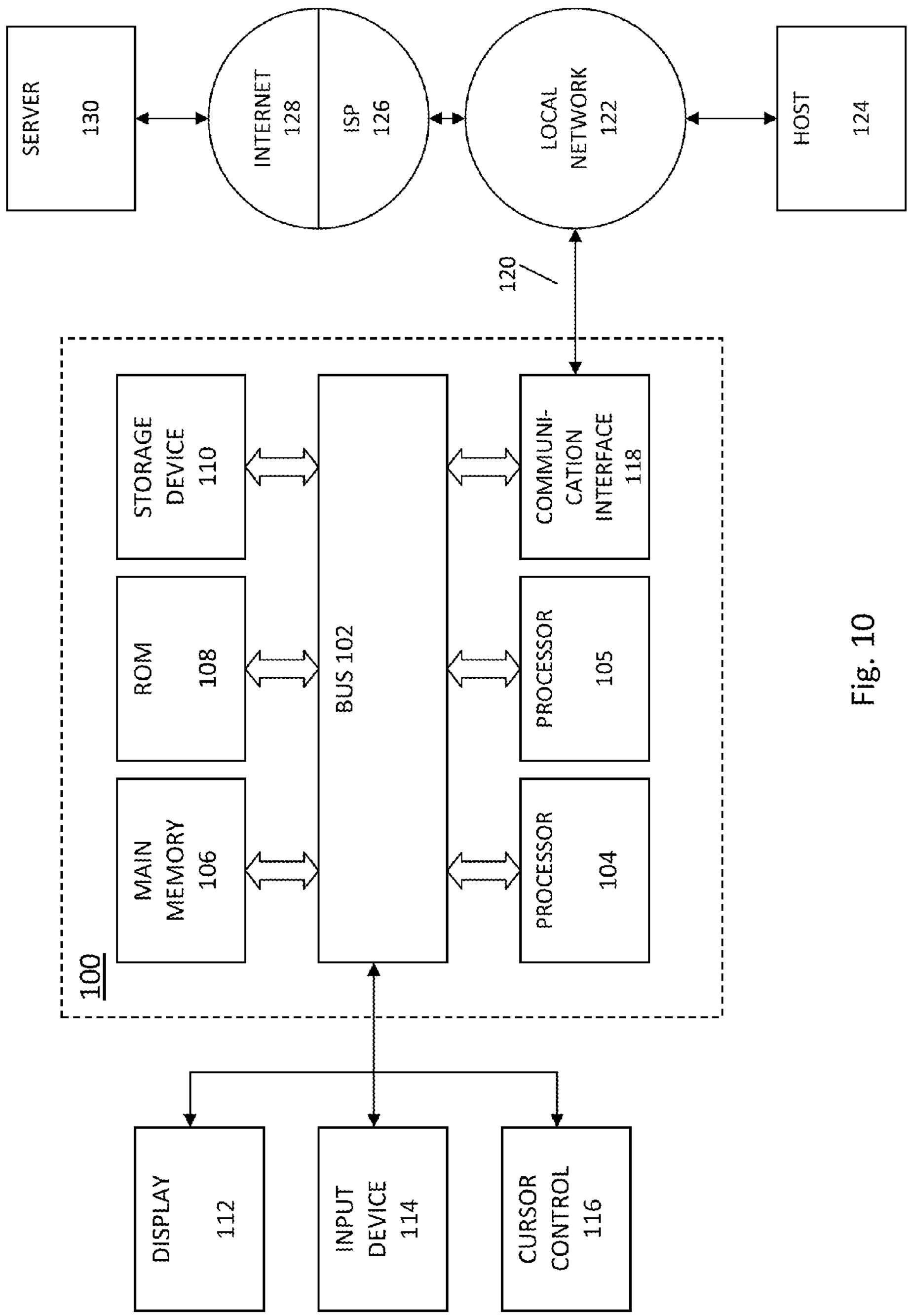

SERVER 130
INTERNET 128
ISP 126
LOCAL NETWORK 122
HOST 124
120
100
STORAGE DEVICE 110
ROM 108
MAIN MEMORY 106
BUS 102
COMMUNI-CATION INTERFACE 118
PROCESSOR 105
PROCESSOR 104
DISPLAY 112
INPUT DEVICE 114
CURSOR CONTROL 116

Fig. 10

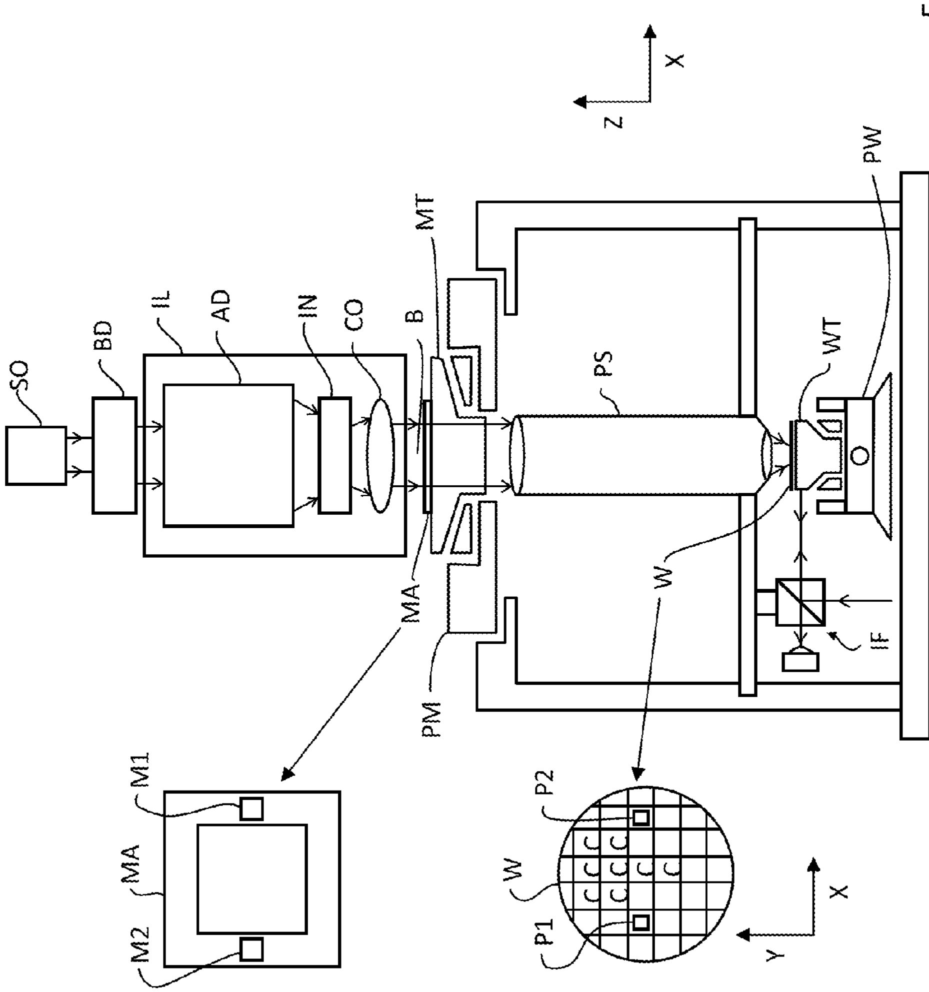


Fig. 11

Fig. 12

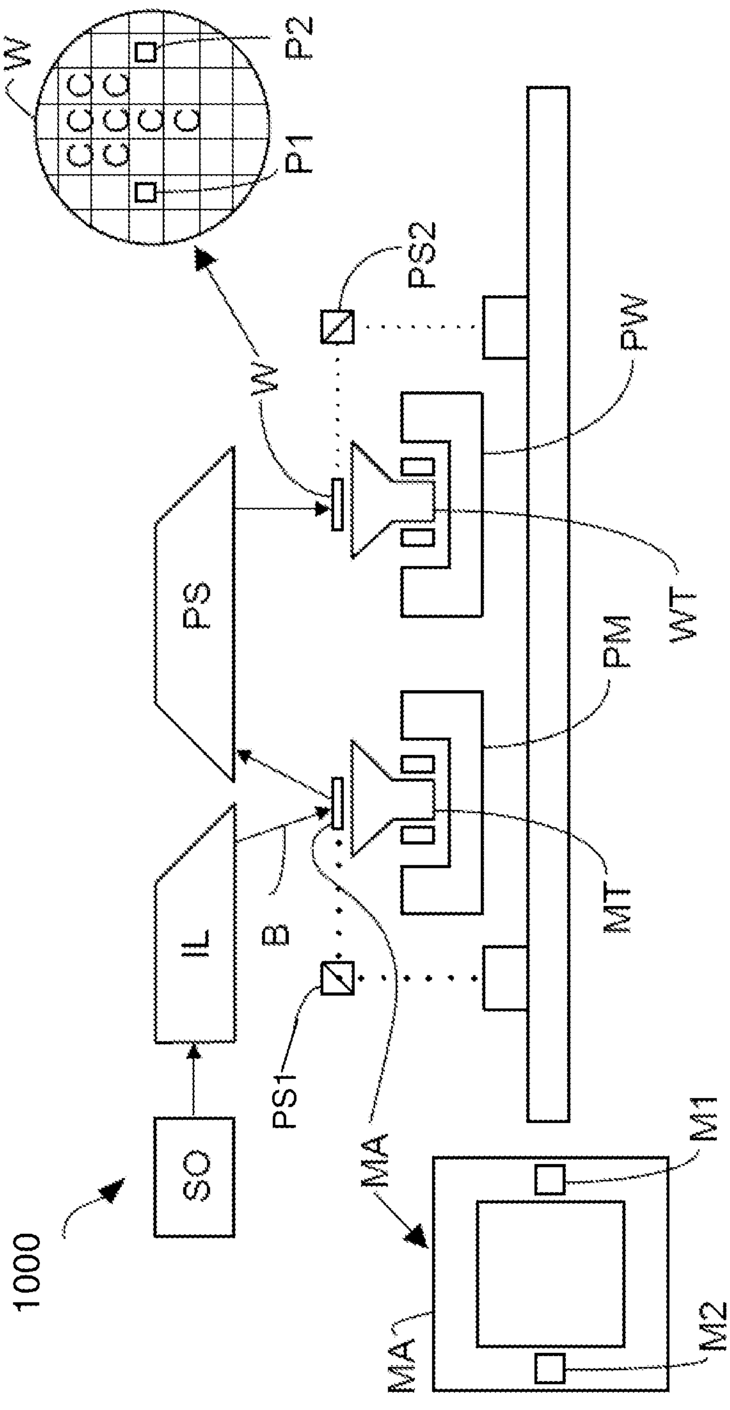
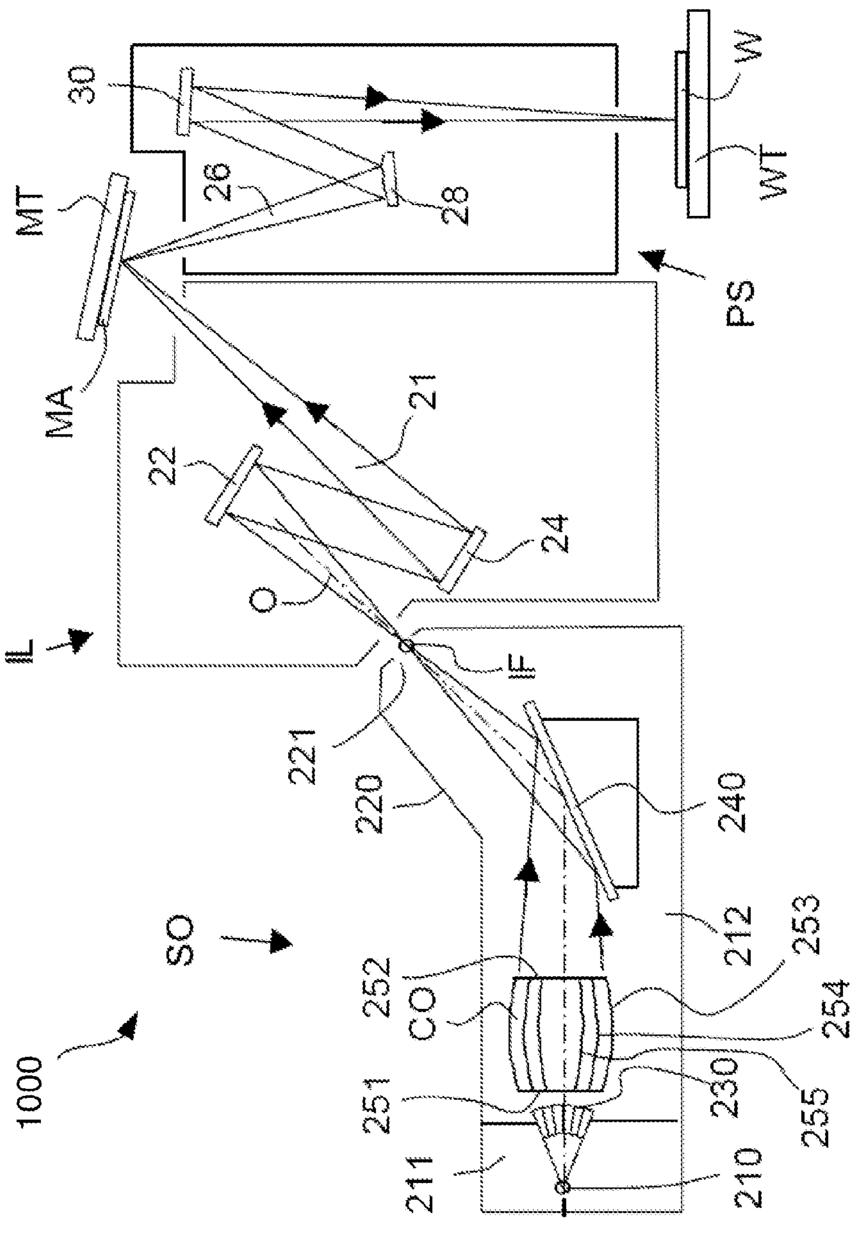


Fig. 13


1000
SO
IL
MA
MT
30
26
28
W
WT
PS
22
21
24
O
IF
221
220
240
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CO
254
230
255
251
211
210

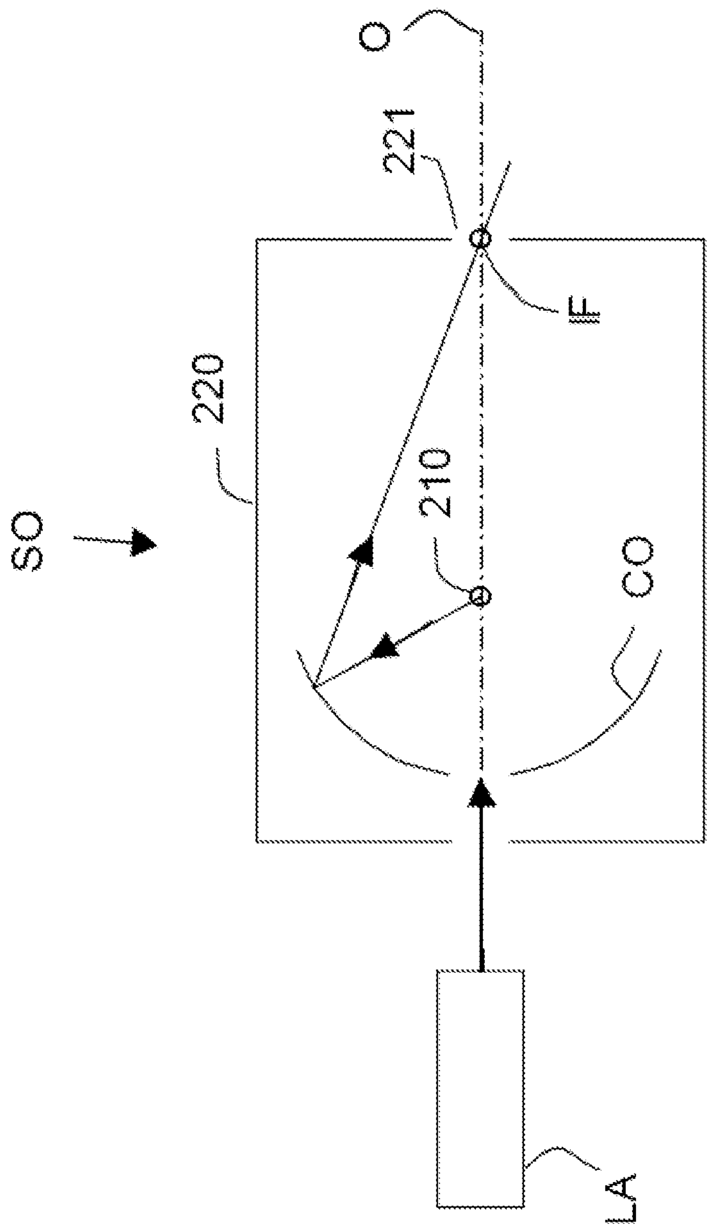

Fig. 14

SOURCE MASK OPTIMIZATION TO REDUCE STOCHASTIC EFFECTS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims priority to U.S. Provisional Application No. 61/585,136 filed on Jan. 10, 2012, which is incorporated herein by reference in its entirety.

TECHNICAL FIELD

The description herein relates to lithographic apparatuses and processes, and more particularly to a tool to optimize an illumination source and/or patterning device/design layout for use in a lithographic apparatus or process.

BACKGROUND

A lithographic projection apparatus can be used, for example, in the manufacture of integrated circuits (ICs). In such a case, a patterning device (e.g., a mask) may contain or provide a circuit pattern corresponding to an individual layer of the IC ("design layout"), and this circuit pattern can be transferred onto a target portion (e.g. comprising one or more dies) on a substrate (e.g., silicon wafer) that has been coated with a layer of radiation-sensitive material ("resist"), by methods such as irradiating the target portion through the circuit pattern on the patterning device. In general, a single substrate contains a plurality of adjacent target portions to which the circuit pattern is transferred successively by the lithographic projection apparatus, one target portion at a time. In one type of lithographic projection apparatuses, the circuit pattern on the entire patterning device is transferred onto one target portion in one go; such an apparatus is commonly referred to as a wafer stepper. In an alternative apparatus, commonly referred to as a step-and-scan apparatus, a projection beam scans over the patterning device in a given reference direction (the "scanning" direction) while synchronously moving the substrate parallel or anti-parallel to this reference direction. Different portions of the circuit pattern on the patterning device are transferred to one target portion progressively. Since, in general, the lithographic projection apparatus will have a magnification factor M (generally <1), the speed F at which the substrate is moved will be a factor M times that at which the projection beam scans the patterning device. More information with regard to lithographic devices as described herein can be gleaned, for example, from U.S. Pat. No. 6,046,792, incorporated herein by reference.

Prior to transferring the circuit pattern from the patterning device to the substrate, the substrate may undergo various procedures, such as priming, resist coating and a soft bake. After exposure, the substrate may be subjected to other procedures, such as a post-exposure bake (PEB), development, a hard bake and measurement/inspection of the transferred circuit pattern. This array of procedures is used as a basis to make an individual layer of a device, e.g., an IC. The substrate may then undergo various processes such as etching, ion-implantation (doping), metallization, oxidation, chemo-mechanical polishing, etc., all intended to finish off the individual layer of the device. If several layers are required in the device, then the whole procedure, or a variant thereof, is repeated for each layer. Eventually, a device will be present in each target portion on the substrate. These devices are then separated from one another by a technique such as dicing or sawing, whence the individual devices can be mounted on a carrier, connected to pins, etc.

As noted, microlithography is a central step in the manufacturing of ICs, where patterns formed on substrates define functional elements of the ICs, such as microprocessors, memory chips etc. Similar lithographic techniques are also used in the formation of flat panel displays, micro-electro mechanical systems (MEMS) and other devices.

As semiconductor manufacturing processes continue to advance, the dimensions of functional elements have continually been reduced while the amount of functional elements, such as transistors, per device has been steadily increasing over decades, following a trend commonly referred to as "Moore's law". At the current state of technology, layers of devices are manufactured using lithographic projection apparatuses that project a design layout onto a substrate using illumination from a deep-ultraviolet illumination source, creating individual functional elements having dimensions well below 100 nm, i.e. less than half the wavelength of the radiation from the illumination source (e.g., a 193 nm illumination source).

This process in which features with dimensions smaller than the classical resolution limit of a lithographic projection apparatus are printed, is commonly known as low-k_1 lithography, according to the resolution formula $CD=k_1 \times \lambda/NA$, where λ is the wavelength of radiation employed (currently in most cases 248 nm or 193 nm), NA is the numerical aperture of projection optics in the lithographic projection apparatus, CD is the "critical dimension"—generally the smallest feature size printed—and k_1 is an empirical resolution factor. In general, the smaller k_1 the more difficult it becomes to reproduce a pattern on the substrate that resembles the shape and dimensions planned by a circuit designer in order to achieve particular electrical functionality and performance. To overcome these difficulties, sophisticated fine-tuning steps are applied to the lithographic projection apparatus and/or design layout. These include, for example, but not limited to, optimization of NA and optical coherence settings, customized illumination schemes, use of phase shifting patterning devices, optical proximity correction (OPC, sometimes also referred to as "optical and process correction") in the design layout, or other methods generally defined as "resolution enhancement techniques" (RET). The term "projection optics" as used herein should be broadly interpreted as encompassing various types of optical systems, including refractive optics, reflective optics, apertures and catadioptric optics, for example. The term "projection optics" may also include components operating according to any of these design types for directing, shaping or controlling the projection beam of radiation, collectively or singularly. The term "projection optics" may include any optical component in the lithographic projection apparatus, no matter where the optical component is located on an optical path of the lithographic projection apparatus. Projection optics may include optical components for shaping, adjusting and/or projecting radiation from the source before the radiation passes the patterning device, and/or optical components for shaping, adjusting and/or projecting the radiation after the radiation passes the patterning device. The projection optics generally exclude the source and the patterning device.

BRIEF SUMMARY

As an example, OPC addresses the fact that the final size and placement of an image of the design layout projected on the substrate will not be identical to, or simply depend only on the size and placement of the design layout on the patterning device. It is noted that the terms "mask", "reticle", "patterning device" are utilized interchangeably herein. Also, person skilled in the art will recognize that, especially in the context of lithography simulation/optimization, the term "mask"/"patterning device" and "design layout" can be used interchangeably, as in lithography simulation/optimization, a physical patterning device is not necessarily used but a design layout can be used to represent a physical patterning device. For the small feature sizes and high feature densities present on some design layout, the position of a particular edge of a given feature will be influenced to a certain extent by the presence or absence of other adjacent features. These proximity effects arise from minute amounts of radiation coupled from one feature to another and/or non-geometrical optical effects such as diffraction and interference. Similarly, proximity effects may arise from diffusion and other chemical effects during post-exposure bake (PEB), resist development, and etching that generally follow lithography.

In order to ensure that the projected image of the design layout is in accordance with requirements of a given target circuit design, proximity effects need to be predicted and compensated for, using sophisticated numerical models, corrections or pre-distortions of the design layout. The article "Full-Chip Lithography Simulation and Design Analysis—How OPC Is Changing IC Design", C. Spence, Proc. SPIE, Vol. 5751, pp 1-14 (2005) provides an overview of current "model-based" optical proximity correction processes. In a typical high-end design almost every feature of the design layout has some modification in order to achieve high fidelity of the projected image to the target design. These modifications may include shifting or biasing of edge positions or line widths as well as application of "assist" features that are intended to assist projection of other features.

Application of model-based OPC to a target design involves good process models and considerable computational resources, given the many millions of features typically present in a chip design. However, applying OPC is generally not an "exact science", but an empirical, iterative process that does not always compensate for all possible proximity effect. Therefore, effect of OPC, e.g., design layouts after application of OPC and any other RET, need to be verified by design inspection, i.e. intensive full-chip simulation using calibrated numerical process models, in order to minimize the possibility of design flaws being built into the patterning device pattern. This is driven by the enormous cost of making high-end patterning devices, which run in the multi-million dollar range, as well as by the impact on turn-around time by reworking or repairing actual patterning devices once they have been manufactured.

Both OPC and full-chip RET verification may be based on numerical modeling systems and methods as described, for example in, U.S. Pat. No. 7,003,758 and an article titled "Optimized Hardware and Software For Fast, Full Chip Simulation", by Y. Cao et al., Proc. SPIE, Vol. 5754, 405 (2005).

One RET is related to adjustment of the global bias of the design layout. The global bias is the difference between the patterns in the design layout and the patterns intended to print on the substrate. For example, a circular pattern of 25 nm diameter may be printed on the substrate by a 50 nm diameter pattern in the design layout or by a 20 nm diameter pattern in the design layout but with high dose.

In addition to optimization to design layouts or patterning devices (e.g., OPC), the illumination source can also be optimized, either jointly with patterning device optimization or separately, in an effort to improve the overall lithography fidelity. The terms "illumination source" and "source" are used interchangeably in this document. Since the 1990s, many off-axis illumination sources, such as annular, quadrupole, and dipole, have been introduced, and have provided more freedom for OPC design, thereby improving the imaging results, As is known, off-axis illumination is a proven way to resolve fine structures (i.e., target features) contained in the patterning device. However, when compared to a traditional illumination source, an off-axis illumination source usually provides less radiation intensity for the aerial image (AI). Thus, it becomes desirable to attempt to optimize the illumination source to achieve the optimal balance between finer resolution and reduced radiation intensity.

Numerous illumination source optimization approaches can be found, for example, in an article by Rosenbluth et al., titled "Optimum Mask and Source Patterns to Print A Given Shape", Journal of Microlithography, Microfabrication, Microsystems 1(1), pp. 13-20, (2002). The source is partitioned into several regions, each of which corresponds to a certain region of the pupil spectrum. Then, the source distribution is assumed to be uniform in each source region and the brightness of each region is optimized for process window. However, such an assumption that the source distribution is uniform in each source region is not always valid, and as a result the effectiveness of this approach suffers. In another example set forth in an article by Granik, titled "Source Optimization for Image Fidelity and Throughput", Journal of Microlithography, Microfabrication, Microsystems 3(4), pp. 509-522, (2004), several existing source optimization approaches are overviewed and a method based on illuminator pixels is proposed that converts the source optimization problem into a series of non-negative least square optimizations. Though these methods have demonstrated some successes, they typically require multiple complicated iterations to converge. In addition, it may be difficult to determine the appropriate/optimal values for some extra parameters, such as γ in Granik's method, which dictates the trade-off between optimizing the source for substrate image fidelity and the smoothness requirement of the source.

For low k_1 photolithography, optimization of both the source and patterning device is useful to ensure a viable process window for projection of critical circuit patterns. Some algorithms (e.g. Socha et. al. Proc. SPIE vol. 5853, 2005, p. 180) discretize illumination into independent source points and mask into diffraction orders in the spatial frequency domain, and separately formulate a cost function (which is defined as a function of selected design variables) based on process window metrics such as exposure latitude which could be predicted by optical imaging models from source point intensities and patterning device diffraction orders. The term "design variables" as used herein comprises a set of parameters of a lithographic projection apparatus, for example, parameters a user of the lithographic projection apparatus can adjust. It should be appreciated that any characteristics of a lithographic projection process, including those of the source, the patterning device, the projection optics, and/or resist characteristics can be among the design variables in the optimization. The cost function is often a non-linear function of the design variables. Then standard optimization techniques are used to minimize the cost function.

Relatedly, the pressure of ever decreasing design rules have driven semiconductor chipmakers to move deeper into the low k_1 lithography era with existing 193 nm ArF lithography. Lithography towards lower k_1 puts heavy demands on RET, exposure tools, and the need for litho-friendly design. 1.35 ArF hyper numerical aperture (NA) exposure tools may be used in the future. To help ensure that circuit design can be produced on to the substrate with workable process window, source-patterning device optimization (referred to herein as source-mask optimization or SMO) is becoming a significant RET for 2×nm node.

A source and patterning device (design layout) optimization method and system that allows for simultaneous optimization of the source and patterning device using a cost function without constraints and within a practicable amount of time is described in a commonly assigned International Patent Application No. PCT/US2009/065359, filed on Nov. 20, 2009, and published as WO2010/059954, titled "Fast Freeform Source and Mask Co-Optimization Method", which is hereby incorporated by reference in its entirety.

Another source and mask optimization method and system that involves optimizing the source by adjusting pixels of the source is described in a commonly assigned U.S. patent application Ser. No. 12/813,456, filed on Jun. 10, 2010, and published as U.S. Patent Application Publication No. 2010/0315614, titled "Source-Mask Optimization in Lithographic Apparatus", which is hereby incorporated by reference in its entirety.

Disclosed herein is a computer-implemented method for improving a lithographic process for imaging a portion of a design layout onto a substrate using a lithographic projection apparatus, the method comprising defining a multi-variable cost function, the multi-variable cost function being a function of one or more stochastic effects of the lithographic process, the one or more stochastic effects being functions of a plurality of design variables that are characteristics of the lithographic process; and reconfiguring one or more of the characteristics of the lithographic process by adjusting one or more of the design variables until a certain termination condition is satisfied. Here, the multi-variable cost function being a function of one or more stochastic effects of the lithographic process does not exclude that the multi-variable cost function may be a function of other variables at the same time.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of various subsystems of a lithography system.

FIG. **2** is a block diagram of simulation models corresponding to the subsystems in FIG. **1**.

FIG. **3** is a flow diagram illustrating aspects of an example methodology of joint optimization.

FIG. **4** shows an embodiment of another optimization method, according to an embodiment.

FIG. **5** shows close matching of the Eq. 7 to the result from rigorous modeling.

FIG. **6** shows prediction of LWRs using the model in Eq. 7 under several illumination conditions of the lithographic projection apparatus.

FIGS. **7**A, **7**B and **8** show example flowcharts of various optimization processes.

FIG. **9** shows an exemplary result from optimization according to an embodiment.

FIG. **10** is a block diagram of an example computer system.

FIG. **11** is a schematic diagram of a lithographic projection apparatus.

FIG. **12** is a schematic diagram of another lithographic projection apparatus.

FIG. **13** is a more detailed view of the apparatus in FIG. **12**.

FIG. **14** is a more detailed view of the source collector module SO of the apparatus of FIGS. **12** and **13**.

DETAILED DESCRIPTION

Although specific reference may be made in this text to the manufacture of ICs, it should be explicitly understood that the description herein has many other possible applications. For example, it may be employed in the manufacture of integrated optical systems, guidance and detection patterns for magnetic domain memories, liquid-crystal display panels, thin-film magnetic heads, etc. The skilled artisan will appreciate that, in the context of such alternative applications, any use of the terms "reticle", "wafer" or "die" in this text should be considered as interchangeable with the more general terms "mask", "substrate" and "target portion", respectively.

In the present document, the terms "radiation" and "beam" are used to encompass all types of electromagnetic radiation, including ultraviolet radiation (e.g. with a wavelength of 365, 248, 193, 157 or 126 nm) and EUV (extreme ultra-violet radiation, e.g. having a wavelength in the range 5-20 nm).

The term "optimizing" and "optimization" as used herein mean adjusting a lithographic projection apparatus such that results and/or processes of lithography have more desirable characteristics, such as higher accuracy of projection of design layouts on a substrate, larger process windows, etc.

Further, the lithographic projection apparatus may be of a type having two or more substrate tables (and/or two or more patterning device tables). In such "multiple stage" devices the additional tables may be used in parallel, or preparatory steps may be carried out on one or more tables while one or more other tables are being used for exposures. Twin stage lithographic projection apparatuses are described, for example, in U.S. Pat. No. 5,969,441, incorporated herein by reference.

The patterning device referred to above comprises or can form design layouts. The design layouts can be generated utilizing CAD (computer-aided design) programs, this process often being referred to as EDA (electronic design automation). Most CAD programs follow a set of predetermined design rules in order to create functional design layouts/patterning devices. These rules are set by processing and design limitations. For example, design rules define the space tolerance between circuit devices (such as gates, capacitors, etc.) or interconnect lines, so as to ensure that the circuit devices or lines do not interact with one another in an undesirable way. The design rule limitations are typically referred to as "critical dimensions" (CD). A critical dimension of a circuit can be defined as the smallest width of a line or hole or the smallest space between two lines or two holes. Thus, the CD determines the overall size and density of the designed circuit. Of course, one of the goals in integrated circuit fabrication is to faithfully reproduce the original circuit design on the substrate (via the patterning device).

The term "mask" or "patterning device" as employed in this text may be broadly interpreted as referring to a generic patterning device that can be used to endow an incoming radiation beam with a patterned cross-section, corresponding to a pattern that is to be created in a target portion of the substrate; the term "light valve" can also be used in this context. Besides the classic mask (transmissive or reflective; binary, phase-shifting, hybrid, etc.), examples of other such patterning devices include:

- a programmable mirror array. An example of such a device is a matrix-addressable surface having a viscoelastic control layer and a reflective surface. The basic principle behind such an apparatus is that (for example) addressed areas of the reflective surface reflect incident radiation as diffracted radiation, whereas unaddressed areas reflect incident radiation as undiffracted radiation. Using an appropriate filter, the said undiffracted radiation can be filtered out of the reflected beam, leaving only the diffracted radiation behind; in this manner, the beam becomes patterned according to the addressing pattern of the matrix-addressable surface. The required matrix addressing can be performed using suitable electronic means. More information on such mirror arrays can be gleaned, for example, from U.S. Pat. Nos. 5,296,891 and 5,523,193, which are incorporated herein by reference.

a programmable LCD array. An example of such a construction is given in U.S. Pat. No. 5,229,872, which is incorporated herein by reference.

As a brief introduction, FIG. **1** illustrates an exemplary lithographic projection apparatus **10**A. Major components are a radiation source **12**A, which may be a deep-ultraviolet excimer laser source or other type of source including an extreme ultra violet (EUV) source (as discussed above, the lithographic projection apparatus itself need not have the radiation source), illumination optics which define the partial coherence (denoted as sigma) and which may include optics **14**A, **16**Aa and **16**Ab that shape radiation from the source **12**A; a patterning device **18**A; and transmission optics **16**Ac that project an image of the patterning device pattern onto a substrate plane **22**A. An adjustable filter or aperture **20**A at the pupil plane of the projection optics may restrict the range of beam angles that impinge on the substrate plane **22**A, where the largest possible angle defines the numerical aperture of the projection optics NA=sin(Θ_{max}).

In an optimization process of a system, a figure of merit of the system can be represented as a cost function. The optimization process boils down to a process of finding a set of parameters (design variables) of the system that minimizes the cost function. The cost function can have any suitable form depending on the goal of the optimization. For example, the cost function can be weighted root mean square (RMS) of deviations of certain characteristics (evaluation points) of the system with respect to the intended values (e.g., ideal values) of these characteristics; the cost function can also be the maximum of these deviations (i.e., worst deviation). The term "evaluation points" herein should be interpreted broadly to include any characteristics of the system. The design variables of the system can be confined to finite ranges and/or be interdependent due to practicalities of implementations of the system. In case of a lithographic projection apparatus, the constraints are often associated with physical properties and characteristics of the hardware such as tunable ranges, and/or patterning device manufacturability design rules, and the evaluation points can include physical points on a resist image on a substrate, as well as non-physical characteristics such as dose and focus.

In a lithographic projection apparatus, a source provides illumination (i.e. light); projection optics direct and shapes the illumination via a patterning device and onto a substrate. The term "projection optics" is broadly defined here to include any optical component that may alter the wavefront of the radiation beam. For example, projection optics may include at least some of the components **14**A, **16**Aa, **16**Ab and **16**Ac. An aerial image (AI) is the radiation intensity distribution at substrate level. A resist layer on the substrate is exposed and the aerial image is transferred to the resist layer as a latent "resist image" (RI) therein. The resist image (RI) can be defined as a spatial distribution of solubility of the resist in the resist layer. A resist model can be used to calculate the resist image from the aerial image, an example of which can be found in commonly assigned U.S. patent application Ser. No. 12/315,849, disclosure of which is hereby incorporated by reference in its entirety. The resist model is related only to properties of the resist layer (e.g., effects of chemical processes which occur during exposure, PEB and development). Optical properties of the lithographic projection apparatus (e.g., properties of the source, the patterning device and the projection optics) dictate the aerial image. Since the patterning device used in the lithographic projection apparatus can be changed, it is desirable to separate the optical properties of the patterning device from the optical properties of the rest of the lithographic projection apparatus including at least the source and the projection optics.

An exemplary flow chart for simulating lithography in a lithographic projection apparatus is illustrated in FIG. **2**. A source model **31** represents optical characteristics (including radiation intensity distribution and/or phase distribution) of the source. A projection optics model **32** represents optical characteristics (including changes to the radiation intensity distribution and/or the phase distribution caused by the projection optics) of the projection optics. A design layout model **35** represents optical characteristics (including changes to the radiation intensity distribution and/or the phase distribution caused by a given design layout **33**) of a design layout, which is the representation of an arrangement of features on or formed by a patterning device. An aerial image **36** can be simulated from the design layout model **35**, the projection optics model **32** and the design layout model **35**. A resist image **37** can be simulated from the aerial image **36** using a resist model **37**. Simulation of lithography can, for example, predict contours and CDs in the resist image.

More specifically, it is noted that the source model **31** can represent the optical characteristics of the source that include, but not limited to, NA-sigma (σ) settings as well as any particular illumination source shape (e.g. off-axis radiation sources such as annular, quadrupole, and dipole, etc.). The projection optics model **32** can represent the optical characteristics of the of the projection optics that include aberration, distortion, refractive indexes, physical sizes, physical dimensions, etc. The design layout model **35** can also represent physical properties of a physical patterning device, as described, for example, in U.S. Pat. No. 7,587,704, which is incorporated by reference in its entirety. The objective of the simulation is to accurately predict, for example, edge placements, aerial image intensity slopes and CDs, which can then be compared against an intended design. The intended design is generally defined as a pre-OPC design layout which can be provided in a standardized digital file format such as GDSII or OASIS or other file format.

From this design layout, one or more portions may be identified, which are referred to as "clips". In an embodiment, a set of clips is extracted, which represents the complicated patterns in the design layout (typically about 50 to 1000 clips, although any number of clips may be used). As will be appreciated by those skilled in the art, these patterns or clips represent small portions (i.e. circuits, cells or patterns) of the design and especially the clips represent small portions for which particular attention and/or verification is needed. In other words, clips may be the portions of the design layout or may be similar or have a similar behavior of portions of the design layout where critical features are identified either by experience (including clips provided by a customer), by trial and error, or by running a full-chip simulation. Clips usually contain one or more test patterns or gauge patterns.

An initial larger set of clips may be provided a priori by a customer based on known critical feature areas in a design layout which require particular image optimization. Alternatively, in another embodiment, the initial larger set of clips may be extracted from the entire design layout by using some kind of automated (such as, machine vision) or manual algorithm that identifies the critical feature areas.

In a lithographic projection apparatus, as an example, a cost function is expressed as

$$CF(z_1, z_2, K, z_N) = \sum_{p=1}^{P} w_p f_p^2(z_1, z_2, K, z_N) \quad \text{(Eq. 1)}$$

wherein (z_1,z_2,K,z_N) are N design variables or values thereof. $f_p(z_1,z_2,K,z_N)$ can be a function of the design variables (z_1, z_2,K,z_N) such as a difference between an actual value and an intended value of a characteristic at an evaluation point for a set of values of the design variables of (z_1,z_2,K,z_N). w_p is a weight constant associated with $f_p(z_1,z_2,K,z_N)$. An evaluation point or pattern more critical than others can be assigned a higher w_p value. Patterns and/or evaluation points with larger number of occurrences may be assigned a higher w_p value, too. Examples of the evaluation points can be any physical point or pattern on the substrate, any point on a virtual design layout, or resist image, or aerial image, or a combination thereof. $f_p(z_1,z_2,K,z_N)$ can also be a function of one or more stochastic effects such as the LWR, which are functions of the design variables (z_1,z_2,K,z_N). The cost function may represent any suitable characteristics of the lithographic projection apparatus or the substrate, for instance, focus, CD, image shift, image distortion, image rotation, stochastic effects, throughput, CDU, or a combination thereof. CDU is local CD variation (e.g., three times of the standard deviation of the local CD distribution). In one embodiment, the cost function represents (i.e., is a function of) CDU, throughput, and the stochastic effects. In one embodiment, the cost function represents (i.e., is a function of) EPE, throughput, and the stochastic effects. In one embodiment, the design variables (z_1, z_2,K,z_N) comprise dose, global bias of the patterning device, shape of illumination from the source, or a combination thereof. Since it is the resist image that often dictates the circuit pattern on a substrate, the cost function often includes functions that represent some characteristics of the resist image. For example, $f_p(z_1,z_2,K,z_N)$ of such an evaluation point can be simply a distance between a point in the resist image to an intended position of that point (i.e., edge placement error $EPE_p(z_1,z_2,K,z_N)$). The design variables can be any adjustable parameters such as adjustable parameters of the source, the patterning device, the projection optics, dose, focus, etc. The projection optics may include components collectively called as "wavefront manipulator" that can be used to adjust shapes of a wavefront and intensity distribution and/or phase shift of the irradiation beam. The projection optics preferably can adjust a wavefront and intensity distribution at any location along an optical path of the lithographic projection apparatus, such as before the patterning device, near a pupil plane, near an image plane, near a focal plane. The projection optics can be used to correct or compensate for certain distortions of the wavefront and intensity distribution caused by, for example, the source, the patterning device, temperature variation in the lithographic projection apparatus, thermal expansion of components of the lithographic projection apparatus. Adjusting the wavefront and intensity distribution can change values of the evaluation points and the cost function. Such changes can be simulated from a model or actually measured. Of course, $CF(z_1,z_2,K,z_N)$ is not limited the form in Eq. 1. $CF(z_1,z_2,K,z_N)$ can be in any other suitable form.

It should be noted that the normal weighted root mean square (RMS) of $f_p(z_1,z_2,K,z_N)$ is defined as

$$\sqrt{\frac{1}{P}\sum_{p=1}^{P} w_p f_p^2(z_1, z_2, K, z_N)},$$

therefore, minimizing the weighted RMS of $f_p(z_1, z_2,K,z_N)$ is equivalent to minimizing the cost function

$$CF(z_1, z_2, K, z_N) = \sum_{p=1}^{P} w_p f_p^2(z_1, z_2, K, z_N),$$

defined in Eq. 1. Thus the weighted RMS of $f_p(z_1, z_2,K,z_N)$ and Eq. 1 may be utilized interchangeably for notational simplicity herein.

Further, if considering maximizing the PW (Process Window), one can consider the same physical location from different PW conditions as different evaluation points in the cost function in (Eq.1). For example, if considering NPW conditions, then one can categorize the evaluation points according to their PW conditions and write the cost functions as:

$$\begin{aligned} CF(z_1, z_2, K, z_N) &= \sum_{p=1}^{P} w_p f_p^2(z_1, z_2, K, z_N) \\ &= \sum_{u=1}^{U} \sum_{p_u=1}^{P_u} w_{p_u} f_{p_u}^2(z_1, z_2, K, z) \end{aligned} \quad \text{(Eq. 1')}$$

Where $f_{p_u}(z_1, z_2,K,z_N)$ is the value of $f_p(z_1,z_2,K,z_N)$ under the u-th PW condition u=1,K,U. When $f_p(z_1,z_2,K,z_N)$ is the EPE, then minimizing the above cost function is equivalent to minimizing the edge shift under various PW conditions, thus this leads to maximizing the PW. In particular, if the PW also consists of different mask bias, then minimizing the above cost function also includes the minimization of MEEF (Mask Error Enhancement Factor), which is defined as the ratio between the substrate EPE and the induced mask edge bias.

The design variables may have constraints, which can be expressed as $(z_1, z_2, \ldots, z_N) \in Z$, where Z is a set of possible values of the design variables. One possible constraint on the design variables may be imposed by a desired throughput of the lithographic projection apparatus. The desired throughput may limit the dose and thus has implications for the stochastic effects (e.g., imposing a lower bound on the stochastic effects). Higher throughput generally leads to lower dose, shorter exposure time and greater stochastic effects. Consideration of substrate throughput and minimization of the stochastic effects may constrain the possible values of the design variables because the stochastic effects are function of the design variables. Without such a constraint imposed by the desired throughput, the optimization may yield a set of values of the design variables that are unrealistic. For example, if the dose is among the design variables, without such a constraint, the optimization may yield a dose value that makes the throughput economically impossible. However, the usefulness of constraints should not be interpreted as a necessity.

The optimization process therefore is to find a set of values of the design variables, under the constraints $(z_1, z_2,K,z_N) \in Z$, that minimize the cost function, i.e., to find

$$(\tilde{z}_1, \tilde{z}_2, K, \tilde{z}_N) = \underset{(z_1,z_2,K,z_N)\in Z}{\arg\min}\ CF(z_1, z_2, K, z_N) = \underset{(z_1,z_2,K,z_N)\in Z}{\arg\min} \sum_{p=1}^{P} w_p f_p^2(z_1, z_2, K, z_N) \quad \text{(Eq. 2)}$$

A general method of optimizing the lithography projection apparatus, according to an embodiment, is illustrated in FIG. **3**. This method comprises a step **302** of defining a multi-variable cost function of a plurality of design variables. The design variables may comprise any suitable combination selected from characteristics of the illumination source (**300**A) (e.g., pupil fill ratio, namely percentage of radiation of the source that passes through a pupil or aperture), characteristics of the projection optics (**300**B) and characteristics of the design layout (**300**C). For example, the design variables may include characteristics of the illumination source (**300**A) and characteristics of the design layout (**300**C) (e.g., global bias) but not characteristics of the projection optics (**300**B), which leads to an SMO. Alternatively, the design variables may include characteristics of the illumination source (**300**A), characteristics of the projection optics (**300**B) and characteristics of the design layout (**300**C), which leads to a source-mask-lens optimization (SMLO). In step **304**, the design variables are simultaneously adjusted so that the cost function is moved towards convergence. In step **306**, it is determined whether a predefined termination condition is satisfied. The predetermined termination condition may include various possibilities, i.e. the cost function may be minimized or maximized, as required by the numerical technique used, the value of the cost function has been equal to a threshold value or has crossed the threshold value, the value of the cost function has reached within a preset error limit, or a preset number of iteration is reached. If either of the conditions in step **306** is satisfied, the method ends. If none of the conditions in step **306** is satisfied, the step **304** and **306** are iteratively repeated until a desired result is obtained.

In a lithographic projection apparatus, the source, patterning device and projection optics can be optimized alternatively (referred to as Alternative Optimization) or optimized simultaneously (referred to as Simultaneous Optimization). The terms "simultaneous", "simultaneously", "joint" and "jointly" as used herein mean that the design variables of the characteristics of the source, patterning device, projection optics and/or any other design variables, are allowed to change at the same time. The term "alternative" and "alternatively" as used herein mean that not all of the design variables are allowed to change at the same time.

In FIG. **3**, the optimization of all the design variables is executed simultaneously. Such flow may be called the simultaneous flow or co-optimization flow. Alternatively, the optimization of all the design variables is executed alternatively, as illustrated in FIG. **4**. In this flow, in each step, some design variables are fixed while the other design variables are optimized to minimize the cost function; then in the next step, a different set of variables are fixed while the others are optimized to minimize the cost function. These steps are executed alternatively until convergence or certain terminating conditions are met. As shown in the non-limiting example flowchart of FIG. **4**, first, a design layout (step **402**) is obtained, then a step of source optimization is executed in step **404**, where all the design variables of the illumination source are optimized (SO) to minimize the cost function while all the other design variables are fixed. Then in the next step **406**, a mask optimization (MO) is performed, where all the design variables of the patterning device are optimized to minimize the cost function while all the other design variables are fixed. These two steps are executed alternatively, until certain terminating conditions are met in step **408**. Various termination conditions can be used, such as, the value of the cost function becomes equal to a threshold value, the value of the cost function crosses the threshold value, the value of the cost function reaches within a preset error limit, or a preset number of iteration is reached, etc. Note that SO-MO-Alternative-Optimization is used as an example for the alternative flow. The alternative flow can take many different forms, such as SO-LO-MO-Alternative-Optimization, where SO, LO (Lens Optimization) is executed, and MO alternatively and iteratively; or first SMO can be executed once, then execute LO and MO alternatively and iteratively; and so on. Finally the output of the optimization result is obtained in step **410**, and the process stops.

The pattern selection algorithm, as discussed before, may be integrated with the simultaneous or alternative optimization. For example, when an alternative optimization is adopted, first a full-chip SO can be performed, the 'hot spots' and/or 'warm spots' are identified, then an MO is performed. In view of the present disclosure numerous permutations and combinations of sub-optimizations are possible in order to achieve the desired optimization results.

FIG. **7**A shows one exemplary method of optimization, where a cost function is minimized. In step **502**, initial values of design variables are obtained, including their tuning ranges, if any. In step S**504**, the multi-variable cost function is set up. In step S**506**, the cost function is expanded within a small enough neighborhood around the starting point value of the design variables for the first iterative step (i=0). In step S**508**, standard multi-variable optimization techniques are applied to minimize the cost function. Note that the optimization problem can apply constraints, such as tuning ranges, during the optimization process in S**508** or at a later stage in the optimization process. Step S**520** indicates that each iteration is done for the given test patterns (also known as "gauges") for the identified evaluation points that have been selected to optimize the lithographic process. In step S**510**, a lithographic response is predicted. In step S**512**, the result of step S**510** is compared with a desired or ideal lithographic response value obtained in step S**522**. If the termination condition is satisfied in step S**514**, i.e. the optimization generates a lithographic response value sufficiently close to the desired value, and then the final value of the design variables is outputted in step S**518**. The output step may also include outputting other functions using the final values of the design variables, such as outputting an wavefront aberration-adjusted map at the pupil plane (or other planes), an optimized source map, and optimized design layout etc. If the termination condition is not satisfied, then in step S**516**, the values of the design variables is updated with the result of the i-th iteration, and the process goes back to step S**506**. The process of FIG. **7**A is elaborated in details below.

In an exemplary optimization process, no relationship between the design variables (z_1, z_2, K, z_N) and $f_p(z_1, z_2, K, z_N)$ is assumed or approximated, except that $f_p(z_1, z_2, K, z_N)$ is sufficiently smooth (e.g. first order derivatives

$$\frac{\partial f_p(z_1, z_2, K, z_N)}{\partial z_n},$$

(n=1,2,K N) exist), which is generally valid in a lithographic projection apparatus. An algorithm, such as the Gauss-Newton algorithm, the Levenberg-Marquardt algorithm, the gradient descent algorithm, simulated annealing, the genetic algorithm, can be applied to find $(\tilde{z}_1,\tilde{z}_2,K\ \tilde{z}_N)$.

Here, the Gauss-Newton algorithm is used as an example. The Gauss-Newton algorithm is an iterative method applicable to a general non-linear multi-variable optimization problem. In the i-th iteration wherein the design variables (z_1,z_2,K,z_N) take values of (z_{1i},z_{2i},K,z_{Ni}), the Gauss-Newton algorithm linearizes $f_p(z_1, z_2,K,z_N)$ in the vicinity of (z_{1i},z_{2i},K,z_{Ni}), and then calculates values $(z_{1(i+1)},z_{2(i+1)},K,z_{N(i+1)})$ in the vicinity of (z_{1i},z_{2i},K,z_{Ni}) that give a minimum of $CF(z_1, z_2,K,z_N)$. The design variables (z_1,z_2,K,z_N) take the values of $(z_{1(i+1)},z_{2(i+1)},K,z_{N(i+1)})$ in the (i+1)-th iteration. This iteration continues until convergence (i.e. $CF(z_1,z_2,K,z_N)$ does not reduce any further) or a preset number of iterations is reached.

Specifically, in the i-th iteration, in the vicinity of (z_{1i},z_{2i},K,z_{Ni}),

$$f_p(z_1, z_2, K, z_N) \approx f_p(z_{1i}, z_{2i}, K, z_{Ni}) + \sum_{n=1}^{N} \frac{\partial f_p(z_1, z_2, K, z_N)}{\partial z_n}\bigg|_{z_1=z_{1i}, z_2=z_{2i}, K, z_N=z_{Ni},} (z_n - z_{ni}) \quad \text{(Eq. 3)}$$

Under the approximation of Eq. 3, the cost function becomes:

$$\begin{aligned} CF(z_1, z_2, K, z_N) &= \sum_{p=1}^{P} w_p f_p^2(z_1, z_2, K, z_N) \\ &= \sum_{p=1}^{P} w_p \Big(f_p(z_{1i}, z_{2i}, K, z_{Ni}) + \sum_{n=1}^{N} \frac{\partial f_p(z_1, z_2, K, z_N)}{\partial z_n}\bigg|_{z_1=z_{1i}, z_2=z_{2i}, K, z_N=z_{Ni},} (z_n - z_{ni}) \Big)^2 \end{aligned} \quad \text{(Eq. 4)}$$

which is a quadratic function of the design variables (z_1,z_2,K,z_N). Every term is constant except the design variables (z_1,z_2,K,z_N).

If the design variables (z_1,z_2,K,z_N) are not under any constraints, $(z_{1(i+1)},z_{2(i+1)},K,z_{N(i+1)})$ can be derived by solving by N linear equations:

$$\frac{\partial CF(z_1, z_2, K, z_N)}{\partial z_n} = 0,$$

wherein n=1,2,K N

If the design variables (z_1,z_2,K,z_N) are under the constraints in the form of J inequalities (e.g. tuning ranges of (z_1,z_2,K,z_N))

$$\sum_{n=1}^{N} A_{nj} z_n \le B_j,$$

for j=1,2,K J; and K equalities (e.g. interdependence between the design variables)

$$\sum_{n=1}^{N} C_{nk} z_n = D_k,$$

for k=1,2,K K; the optimization process becomes a classic quadratic programming problem, wherein A_{nj}, B_j, C_{nk}, D_k are constants. Additional constraints can be imposed for each iteration. For example, a "damping factor" Δ_D can be introduced to limit the difference between $(z_{1(i+1)},z_{2(i+1)},K,z_{N(i+1)})$ and (z_{1i},z_{2i},K,z_{Ni}), so that the approximation of Eq. 3 holds. Such constraints can be expressed as $z_{ni}-\Delta_D \le z_n \le z_{ni}+\Delta_D$. $(z_{1(i+1)},z_{2(i+1)},K,z_{N(i+1)})$ can be derived using, for example, methods described in Numerical Optimization (2nd ed.) by Jorge Nocedal and Stephen J. Wright (Berlin NeW York: Vandenberghe. Cambridge University Press).

Instead of minimizing the RMS of $f_p(z_1,z_2,K,z_N)$, the optimization process can minimize magnitude of the largest deviation (the worst defect) among the evaluation points to their intended values. In this approach, the cost function can alternatively be expressed as

$$CF(z_1, z_2, K, z_N) = \max_{1 \le p \le P} \frac{f_p(z_1, z_2, K, z_N)}{CL_p}, \quad \text{(Eq. 5)}$$

wherein CL_p is the maximum allowed value for $f_p(z_1, z_2,K,z_N)$. This cost function represents the worst defect among the evaluation points. Optimization using this cost function minimizes magnitude of the worst defect. An iterative greedy algorithm can be used for this optimization.

The cost function of Eq. 5 can be approximated as:

$$CF(z_1, z_2, K, z_N) = \sum_{p=1}^{P} \left(\frac{f_p(z_1, z_2, K, z_N)}{CL_p} \right)^q, \quad \text{(Eq. 6)}$$

wherein q is an even positive integer such as at least 4, preferably at least 10. Eq. 6 mimics the behavior of Eq. 5, while allowing the optimization to be executed analytically and accelerated by using methods such as the deepest descent method, the conjugate gradient method, etc.

Minimizing the worst defect size can also be combined with linearizing of $f_p(z_1,z_2,K,z_N)$. Specifically, $f_p(z_1,z_2,K,z_N)$ is approximated as in Eq. 3. Then the constraints on worst defect size are written as inequalities $E_{Lp} \le f_p(z_1,z_2,K,z_N) \le E_{Up}$, wherein E_{Lp} and E_{Up} are two constants specifying the minimum and maximum allowed deviation for the $f_p(z_1,z_2,K,z_N)$. Plugging Eq. 3 in, these constraints are transformed to, for p=1, . . . P,

$$\sum_{n=1}^{N} \frac{\partial f_p(z_1, z_2, K, z_N)}{\partial z_n}\bigg|_{z_1=z_{1i}, z_2=z_{2i}, K, z_N=z_{Ni},} z_n \le E_{Up} + \sum_{n=1}^{N} \frac{\partial f_p(z_1, z_2, K, z_N)}{\partial z_n}\bigg|_{z_1=z_{1i}, z_2=z_{2i}, K, z_N=z_{Ni},} z_{ni} - f_p(z_{1i}, z_{2i}, K, z_{Ni}) \quad \text{(Eq. 6')}$$

and

-continued

$$-\sum_{n=1}^{N}\left.\frac{\partial f_p(z_1,z_2,K,z_N)}{\partial z_n}\right|_{z_1=z_{1i},z_2=z_{2i},K,z_N=z_{Ni},} z_n \le -E_{Up}-\sum_{n=1}^{N}\left.\frac{\partial f_p(z_1,z_2,K,z_N)}{\partial z_n}\right|_{z_1=z_{1i},z_2=z_{2i},K,z_N=z_{Ni},} z_{ni}+f_p(z_{1i},z_{2i},K,z_{Ni}) \quad \text{(Eq. 6'')}$$

Since Eq. 3 is generally valid only in the vicinity of $(z_{1i}, z_{2i}, K, z_{Ni})$, in case the desired constraints $E_{Lp} \le f_p(z_1,z_2,K,z_N) \le E_{Up}$ cannot be achieved in such vicinity, which can be determined by any conflict among the inequalities, the constants E_{Lp} and E_{Up} can be relaxed until the constraints are achievable. This optimization process minimizes the worst defect size in the vicinity of (z_{1i},z_{2i},K,z_{Ni}). Then each step reduces the worst defect size gradually, and each step is executed iteratively until certain terminating conditions are met. This will lead to optimal reduction of the worst defect size.

Another way to minimize the worst defect is to adjust the weight w_p in each iteration. For example, after the i-th iteration, if the r-th evaluation point is the worst defect, w_r can be increased in the (i+1)-th iteration so that the reduction of that evaluation point's defect size is given higher priority.

In addition, the cost functions in Eq.4 and Eq.5 can be modified by introducing a Lagrange multiplier to achieve compromise between the optimization on RMS of the defect size and the optimization on the worst defect size, i.e.,

$$CF(z_1,z_2,K,z_N) = (1-\lambda)\sum_{p=1}^{P} w_p f_p^2(z_1,z_2,K,z_N) + \lambda \max_{1\le p\le P}\frac{f_p(z_1,z_2,K,z_N)}{CL_p} \quad \text{(Eq. 6''')}$$

where λ is a preset constant that specifies the trade-off between the optimization on RMS of the defect size and the optimization on the worst defect size. In particular, if $\lambda=0$, then this becomes Eq.4 and the RMS of the defect size is only minimized; while if $\lambda=1$, then this becomes Eq.5 and the worst defect size is only minimized; if $0<\lambda<1$, then both are taken into consideration in the optimization. Such optimization can be solved using multiple methods. For example, the weighting in each iteration may be adjusted, similar to the one described previously. Alternatively, similar to minimizing the worst defect size from inequalities, the inequalities of Eq. 6' and 6" can be viewed as constraints of the design variables during solution of the quadratic programming problem. Then, the bounds on the worst defect size can be relaxed incrementally or increase the weight for the worst defect size incrementally, compute the cost function value for every achievable worst defect size, and choose the design variable values that minimize the total cost function as the initial point for the next step. By doing this iteratively, the minimization of this new cost function can be achieved.

In a lithographic projection apparatus, for example, using an EUV (extreme ultra-violet radiation, e.g. having a wavelength in the range 5-20 nm) source or a non-EUV source reduced radiation intensity may lead to stronger stochastic effects, such as pronounced line width roughness (LWR) and local CD variation in small two-dimensional features such as holes. In a lithographic projection apparatus using an EUV source, reduced radiation intensity may be attributed to low total radiation output from the source, radiation loss from optics that shape the radiation from the source, transmission loss through the projection optics, high photon energy that leads to fewer photons under a constant dose, etc. The stochastic effects may be attributed to factors such as photon shot noise, photon-generated secondary electrons, photon-generated acids in the resist. The small sizes of features for which EUV is called for further compound these stochastic effects. The stochastic effects in smaller features are a significant factor in production yield and justifies inclusion in a variety of optimization processes of the lithographic projection apparatus.

Under the same radiation intensity, lower exposure time of each substrate leads to higher throughput of a lithographic projection apparatus but stronger stochastic effect. The photon shot noise in a given feature under a given radiation intensity is proportional to the square root of the exposure time. The desire to lower exposure time for the purpose of increasing the throughput exists in lithography using EUV and other radiation sources. Therefore, the methods and apparatuses described herein that consider the stochastic effect in the optimization process are not limited to EUV lithography.

In one embodiment, the cost function includes at least one $f_p(z_1,z_2,K,z_N)$ that is a function of one or more stochastic effects such as the LWR or local CD variation of 2D features. For example,

$$f_p(z_1,z_2,K,z_N) = \alpha\cdot\sqrt{\left(\frac{\sqrt{N_{Ph}(z_1,z_2,K,z_N)}}{N_{Ph}(z_1,z_2,K,z_N)}\right)^2+\left(\frac{\sqrt{N_{Ac}(z_1,z_2,K,z_N)}}{N_{Ac}(z_1,z_2,K,z_N)}\right)^2}, \quad \text{(Eq. 7)}$$

wherein N_{Ph} is the flux density of photons from the source; N_{Ac} relates to an number density of acids generated in the resist by the photons after base quenching; and α is a coefficient such as dose sensitivity or an empirical factor that matches Eq. 7 to actual LWR of a specific feature in a specific resist. N_{Ph}, and N_{Ac} can be measured, empirically determined, or simulated from various models. The exemplary $f_p(z_1,z_2,K,z_N)$ in Eq. 7 measures LWR of a line feature or CD variation of a 2D feature. Of course, $f_p(z_1,z_2,K,z_N)$ can have any other suitable form that is a function of one or more stochastic effects. In another example, $f_p(z_1,z_2,K,z_N)$ is a function of a combination of one or more stochastic effects and other metrics such as EPE.

FIG. **5** shows close matching of $f_p(z_1,z_2,K,z_N)$ in Eq. 7 to the stochastic effects calculated from rigorous modeling. The rigorous modeling is conducted for lines with 20 nm, 22 nm, 24 nm, 26 nm, 28 nm, 30 nm, and 32 nm half-pitch respectively from upper curve to lower curve for a source with NA=0.33 and with 7 nm resist blur. The rigorous modeling is too computationally expensive during the optimization procedure. In FIG. **5**, the symbols are the LWRs predicted by the rigorous modeling. Different symbols correspond to different dense line half-pitch values. The curves are fittings of Eq. 7 to the result of the rigorous modeling.

FIG. **6** shows prediction of LWRs using the model in Eq. 7 under several illumination conditions of the lithographic projection apparatus (NA=0.25 and NA=0.33) for 27 nm wide lines. Smaller partial coherence factor σ and larger NA yield smaller LWR.

The f_p (z_1,z_2,K,z_N) that is a function of one or more stochastic effects may have other forms such as

$$f_p(z_1, z_2, K, z_N) = \alpha \cdot \sqrt{\left(\frac{\sqrt{N_{Ph}(z_1, z_2, K, z_N)}}{N_{Ph}(z_1, z_2, K, z_N)}\right)^2 + \left(\frac{\sqrt{N_{Ac}(z_1, z_2, K, z_N)}}{N_{Ac}(z_1, z_2, K, z_N)}\right)^2} + h, \quad \text{(Eq. 8)}$$

wherein h is a function of any characteristics of the lithography process, such as the CDU, throughput, EPE, dose.

Optimizing a lithographic projection apparatus can expand the process window. A larger process window provides more flexibility in process design and chip design. The process window can be defined as a set of focus and dose values for which the resist image are within a certain limit of the design target of the resist image. Note that all the methods discussed here may also be extended to a generalized process window definition that can be established by different or additional base parameters in addition to exposure dose and defocus. These may include, but are not limited to, optical settings such as NA, sigma, aberrations, polarization, or optical constants of the resist layer. For example, as described earlier, if the PW also consists of different mask bias, then the optimization includes the minimization of MEEF (Mask Error Enhancement Factor), which is defined as the ratio between the substrate EPE and the induced mask edge bias. The process window defined on focus and dose values only serve as an example in this disclosure. A method of maximizing the process window, according to an embodiment, is described below.

In a first step, starting from a known condition (f_0, ϵ_0) in the process window, wherein f_0 is a nominal focus and ϵ_0 is a nominal dose, minimizing one of the cost functions below in the vicinity $(f_0 \pm \Delta f, \epsilon_0 \pm \Delta\epsilon)$:

$$CF(z_1, z_2, K, z_N, f_0, \varepsilon_0) = \max_{(f,\varepsilon)=(f_0\pm\Delta f, \varepsilon_0\pm\Delta\varepsilon)} \max_p |f_p(z_1, z_2, K, z_N, f, \varepsilon)|. \quad \text{(Eq. 27)}$$

or

$$CF(z_1, z_2, K, z_N, f_0, \varepsilon_0) = \sum_{(f,\varepsilon)=(f_0\pm\Delta f, \varepsilon_0\pm\Delta\varepsilon)} \sum_p w_p f_{p,}^2(z_1, z_2, K, z_N, f, \varepsilon) \quad \text{(Eq. 27')}$$

or

$$CF(z_1, z_2, K, z_N, f_0, \varepsilon_0) = (1-\lambda) \sum_{(f,\varepsilon)=(f_0\pm\Delta f, \varepsilon_0\pm\Delta\varepsilon)} \sum_p w_p f_{p,}^2(z_1, z_2, K, z_N, f, \varepsilon) + \lambda \max_{(f,\varepsilon)=(f_0\pm\Delta f, \varepsilon_0\pm\Delta\varepsilon)} \max_p |f_p(z_1, z_2, K, z_N, f, \varepsilon)| \quad \text{(Eq. 27'')}$$

If the nominal focus f_0 and nominal dose ϵ_0 are allowed to shift, they can be optimized jointly with the design variables (z_1, z_2, K, z_N). In the next step, $(f_0 \pm \Delta f, \epsilon_0 \pm \Delta\epsilon)$ is accepted as part of the process window, if a set of values of $(z_1, z_2, K, z_N, f, \epsilon)$ can be found such that the cost function is within a preset limit.

Alternatively, if the focus and dose are not allowed to shift, the design variables (z_1, z_2, K, z_N) are optimized with the focus and dose fixed at the nominal focus f_0 and nominal dose ϵ_0. In an alternative embodiment, $(f_0 \pm \Delta f, \epsilon_0 \pm \Delta\epsilon)$ is accepted as part of the process window, if a set of values of (z_1, z_2, K, z_N) can be found such that the cost function is within a preset limit.

The methods described earlier in this disclosure can be used to minimize the respective cost functions of Eqs. 27, 27', or 27". If the design variables are characteristics of the projection optics, such as the Zernike coefficients, then minimizing the cost functions of Eqs. 27, 27', or 27" leads to process window maximization based on projection optics optimization, i.e., LO. If the design variables are characteristics of the source and patterning device in addition to those of the projection optics, then minimizing the cost function of Eqs. 27, 27', or 27" leads to process window maximizing based on SMLO, as illustrated in FIG. **3**. If the design variables are characteristics of the source and patterning device and, then minimizing the cost functions of Eqs. 27, 27', or 27" leads to process window maximization based on SMO. The cost functions of Eqs. 27, 27', or 27" can also include at least one $f_p(z_1, z_2, K, z_N)$ such as that in Eq. 7 or Eq. 8, that is a function of one or more stochastic effects such as the LWR or local CD variation of 2D features.

FIG. **8** shows one specific example of how a simultaneous SMLO process can use a Gauss Newton Algorithm for optimization. In step **S702**, starting values of design variables are identified. Tuning ranges for each variable may also be identified. In step **S704**, the cost function is defined using the design variables. In step **S706** cost function is expanded around the starting values for all evaluation points in the design layout. In optional step **S710**, a full-chip simulation is executed to cover all critical patterns in a full-chip design layout. Desired lithographic response metric (such as CD or EPE) is obtained in step **S714**, and compared with predicted values of those quantities in step **S712**. In step **S716**, a process window is determined. Steps **S718**, **S720**, and **S722** are similar to corresponding steps **S514**, **S516** and **S518**, as described with respect to FIG. **7**A. As mentioned before, the final output may be a wavefront aberration map in the pupil plane, optimized to produce the desired imaging performance. The final output may also be an optimized source map and/or an optimized design layout.

FIG. **7**B shows an exemplary method to optimize the cost function where the design variables (z_1, z_2, K, z_N) include design variables that may only assume discrete values.

The method starts by defining the pixel groups of the illumination source and the patterning device tiles of the patterning device (step **802**). Generally, a pixel group or a patterning device tile may also be referred to as a division of a lithographic process component. In one exemplary approach, the illumination source is divided into 117 pixel groups, and 94 patterning device tiles are defined for the patterning device, substantially as described above, resulting in a total of 211 divisions.

In step **804**, a lithographic model is selected as the basis for photolithographic simulation. Photolithographic simulations produce results that are used in calculations of photolithographic metrics, or responses. A particular photolithographic metric is defined to be the performance metric that is to be optimized (step **806**). In step **808**, the initial (pre-optimization) conditions for the illumination source and the patterning device are set up. Initial conditions include initial states for the pixel groups of the illumination source and the patterning device tiles of the patterning device such that references may be made to an initial illumination shape and an initial patterning device pattern. Initial conditions may also include mask bias, NA, and focus ramp range. Although steps **802**, **804**, **806**, and **808** are depicted as sequential steps, it will be appreciated that in other embodiments of the invention, these steps may be performed in other sequences.

In step **810**, the pixel groups and patterning device tiles are ranked. Pixel groups and patterning device tiles may be interleaved in the ranking. Various ways of ranking may be employed, including: sequentially (e.g., from pixel group **1** to pixel group **117** and from patterning device tile **1** to patterning device tile **94**), randomly, according to the physical locations of the pixel groups and patterning device tiles (e.g., ranking pixel groups closer to the center of the illumination source higher), and according to how an alteration of the pixel group or patterning device tile affects the performance metric.

Once the pixel groups and patterning device tiles are ranked, the illumination source and patterning device are adjusted to improve the performance metric (step **812**). In step **812**, each of the pixel groups and patterning device tiles are analyzed, in order of ranking, to determine whether an alteration of the pixel group or patterning device tile will result in an improved performance metric. If it is determined that the performance metric will be improved, then the pixel group or patterning device tile is accordingly altered, and the resulting improved performance metric and modified illumination shape or modified patterning device pattern form the baseline for comparison for subsequent analyses of lower-ranked pixel groups and patterning device tiles. In other words, alterations that improve the performance metric are retained. As alterations to the states of pixel groups and patterning device tiles are made and retained, the initial illumination shape and initial patterning device pattern changes accordingly, so that a modified illumination shape and a modified patterning device pattern result from the optimization process in step **812**.

In other approaches, patterning device polygon shape adjustments and pairwise polling of pixel groups and/or patterning device tiles are also performed within the optimization process of **812**.

In an alternative embodiment the interleaved simultaneous optimization procedure may include to alter a pixel group of the illumination source and if an improvement of the performance metric is found, the dose is stepped up and down to look for further improvement. In a further alternative embodiment the stepping up and down of the dose or intensity may be replaced by a bias change of the patterning device pattern to look for further improvement in the simultaneous optimization procedure.

In step **814**, a determination is made as to whether the performance metric has converged. The performance metric may be considered to have converged, for example, if little or no improvement to the performance metric has been witnessed in the last several iterations of steps **810** and **812**. If the performance metric has not converged, then the steps of **810** and **812** are repeated in the next iteration, where the modified illumination shape and modified patterning device from the current iteration are used as the initial illumination shape and initial patterning device for the next iteration (step **816**).

FIG. **9** shows exemplary LWRs of 27 nm dense vertical lines, with NA=0.33 from a source with fixed annular 0.9/0.2σ aperture (i.e., an aperture source) shown in the upper left panel and from an optimized source whose aperture is shown in the lower left panel. The SMO used a cost function that includes the $f_p(z_1,z_2,K,z_N)$ of Eq. 7 or Eq. 8. As FIG. **9** plainly shows, SMO is effective in reducing LWR (Eq. 7), CDU and their combination (Eq. 8).

The optimization methods described above may be used to increase the throughput of the lithographic projection apparatus. For example, the cost function may include an $f_p(z_1,z_2,K,z_N)$ that is a function of the exposure time. Optimization of such a cost function is preferably constrained or influenced by a measure of the stochastic effects or other metrics. Specifically, a computer-implemented method for increasing a throughput of a lithographic process may include optimizing a cost function that is a function of one or more stochastic effects of the lithographic process and a function of an exposure time of the substrate, in order to minimize the exposure time.

FIG. **10** is a block diagram that illustrates a computer system **100** which can assist in implementing the optimization methods and flows disclosed herein. Computer system **100** includes a bus **102** or other communication mechanism for communicating information, and a processor **104** (or multiple processors **104** and **105**) coupled with bus **102** for processing information. Computer system **100** also includes a main memory **106**, such as a random access memory (RAM) or other dynamic storage device, coupled to bus **102** for storing information and instructions to be executed by processor **104**. Main memory **106** also may be used for storing temporary variables or other intermediate information during execution of instructions to be executed by processor **104**. Computer system **100** further includes a read only memory (ROM) **108** or other static storage device coupled to bus **102** for storing static information and instructions for processor **104**. A storage device **110**, such as a magnetic disk or optical disk, is provided and coupled to bus **102** for storing information and instructions.

Computer system **100** may be coupled via bus **102** to a display **112**, such as a cathode ray tube (CRT) or flat panel or touch panel display for displaying information to a computer user. An input device **114**, including alphanumeric and other keys, is coupled to bus **102** for communicating information and command selections to processor **104**. Another type of user input device is cursor control **116**, such as a mouse, a trackball, or cursor direction keys for communicating direction information and command selections to processor **104** and for controlling cursor movement on display **112**. This input device typically has two degrees of freedom in two axes, a first axis (e.g., x) and a second axis (e.g., y), that allows the device to specify positions in a plane. A touch panel (screen) display may also be used as an input device.

According to one embodiment, portions of the optimization process may be performed by computer system **100** in response to processor **104** executing one or more sequences of one or more instructions contained in main memory **106**. Such instructions may be read into main memory **106** from another computer-readable medium, such as storage device **110**. Execution of the sequences of instructions contained in main memory **106** causes processor **104** to perform the process steps described herein. One or more processors in a multi-processing arrangement may also be employed to execute the sequences of instructions contained in main memory **106**. In an alternative embodiment, hard-wired circuitry may be used in place of or in combination with software instructions. Thus, the description herein is not limited to any specific combination of hardware circuitry and software.

The term "computer-readable medium" as used herein refers to any medium that participates in providing instructions to processor **104** for execution. Such a medium may take many forms, including but not limited to, non-volatile media, volatile media, and transmission media. Non-volatile media include, for example, optical or magnetic disks, such as storage device **110**. Volatile media include dynamic memory, such as main memory **106**. Transmission media include coaxial cables, copper wire and fiber optics, including the wires that comprise bus **102**. Transmission media can also take the form of acoustic or light waves, such as those generated during radio frequency (RF) and infrared (IR) data communications. Common forms of computer-readable media include, for example, a floppy disk, a flexible disk, hard disk, magnetic tape, any other magnetic medium, a CD-ROM, DVD, any other optical medium, punch cards, paper tape, any other physical medium with patterns of holes, a RAM, a PROM, and EPROM, a FLASH-EPROM, any other memory chip or cartridge, a carrier wave as described hereinafter, or any other medium from which a computer can read.

Various forms of computer readable media may be involved in carrying one or more sequences of one or more instructions to processor **104** for execution. For example, the instructions may initially be borne on a magnetic disk of a remote computer. The remote computer can load the instructions into its dynamic memory and send the instructions over a telephone line using a modem. A modem local to computer system **100** can receive the data on the telephone line and use an infrared transmitter to convert the data to an infrared signal. An infrared detector coupled to bus **102** can receive the data carried in the infrared signal and place the data on bus **102**. Bus **102** carries the data to main memory **106**, from which processor **104** retrieves and executes the instructions. The instructions received by main memory **106** may optionally be stored on storage device **110** either before or after execution by processor **104**.

Computer system **100** also preferably includes a communication interface **118** coupled to bus **102**. Communication interface **118** provides a two-way data communication coupling to a network link **120** that is connected to a local network **122**. For example, communication interface **118** may be an integrated services digital network (ISDN) card or a modem to provide a data communication connection to a corresponding type of telephone line. As another example, communication interface **118** may be a local area network (LAN) card to provide a data communication connection to a compatible LAN. Wireless links may also be implemented. In any such implementation, communication interface **118** sends and receives electrical, electromagnetic or optical signals that carry digital data streams representing various types of information.

Network link **120** typically provides data communication through one or more networks to other data devices. For example, network link **120** may provide a connection through local network **122** to a host computer **124** or to data equipment operated by an Internet Service Provider (ISP) **126**. ISP **126** in turn provides data communication services through the worldwide packet data communication network, now commonly referred to as the "Internet" **128**. Local network **122** and Internet **128** both use electrical, electromagnetic or optical signals that carry digital data streams. The signals through the various networks and the signals on network link **120** and through communication interface **118**, which carry the digital data to and from computer system **100**, are exemplary forms of carrier waves transporting the information.

Computer system **100** can send messages and receive data, including program code, through the network(s), network link **120**, and communication interface **118**. In the Internet example, a server **130** might transmit a requested code for an application program through Internet **128**, ISP **126**, local network **122** and communication interface **118**. One such downloaded application may provide for the illumination optimization of the embodiment, for example. The received code may be executed by processor **104** as it is received, and/or stored in storage device **110**, or other non-volatile storage for later execution. In this manner, computer system **100** may obtain application code in the form of a carrier wave.

FIG. **11** schematically depicts an exemplary lithographic projection apparatus whose illumination source could be optimized utilizing the methods described herein. The apparatus comprises:

an illumination system IL, to condition a beam B of radiation. In this particular case, the illumination system also comprises a radiation source SO;

a first object table (e.g., mask table) MT provided with a patterning device holder to hold a patterning device MA (e.g., a reticle), and connected to a first positioner to accurately position the patterning device with respect to item PS;

a second object table (substrate table) WT provided with a substrate holder to hold a substrate W (e.g., a resist-coated silicon wafer), and connected to a second positioner to accurately position the substrate with respect to item PS;

a projection system ("lens") PS (e.g., a refractive, catoptric or catadioptric optical system) to image an irradiated portion of the patterning device MA onto a target portion C (e.g., comprising one or more dies) of the substrate W.

As depicted herein, the apparatus is of a transmissive type (i.e., has a transmissive mask). However, in general, it may also be of a reflective type, for example (with a reflective mask). Alternatively, the apparatus may employ another kind of patterning device as an alternative to the use of a classic mask; examples include a programmable mirror array or LCD matrix.

The source SO (e.g., a mercury lamp or excimer laser) produces a beam of radiation. This beam is fed into an illumination system (illuminator) IL, either directly or after having traversed conditioning means, such as a beam expander Ex, for example. The illuminator IL may comprise adjusting means AD for setting the outer and/or inner radial extent (commonly referred to as σ-outer and σ-inner, respectively) of the intensity distribution in the beam. In addition, it will generally comprise various other components, such as an integrator IN and a condenser CO. In this way, the beam B impinging on the patterning device MA has a desired uniformity and intensity distribution in its cross-section.

It should be noted with regard to FIG. **11** that the source SO may be within the housing of the lithographic projection apparatus (as is often the case when the source SO is a mercury lamp, for example), but that it may also be remote from the lithographic projection apparatus, the radiation beam that it produces being led into the apparatus (e.g., with the aid of suitable directing mirrors); this latter scenario is often the case when the source SO is an excimer laser (e.g., based on KrF, ArF or F_2 lasing).

The beam B subsequently intercepts the patterning device MA, which is held on a patterning device table MT. Having traversed the patterning device MA, the beam B passes through the lens PL, which focuses the beam B onto a target portion C of the substrate W. With the aid of the second positioning means (and interferometric measuring means IF), the substrate table WT can be moved accurately, e.g. so as to position different target portions C in the path of the beam B. Similarly, the first positioning means can be used to accurately position the patterning device MA with respect to the path of the beam B, e.g., after mechanical retrieval of the patterning device MA from a patterning device library, or during a scan. In general, movement of the object tables MT, WT will be realized with the aid of a long-stroke module (coarse positioning) and a short-stroke module (fine positioning), which are not explicitly depicted in FIG. **11**. However, in the case of a wafer stepper (as opposed to a step-and-scan tool) the patterning device table MT may just be connected to a short stroke actuator, or may be fixed.

The depicted tool can be used in two different modes:

In step mode, the patterning device table MT is kept essentially stationary, and an entire patterning device image is projected in one go (i.e., a single "flash") onto a target portion C. The substrate table WT is then shifted in the x and/or y directions so that a different target portion C can be irradiated by the beam B;

In scan mode, essentially the same scenario applies, except that a given target portion C is not exposed in a single "flash". Instead, the patterning device table MT is movable in a given direction (the so-called "scan direction", e.g., the y direction) with a speed v, so that the projection beam B is caused to scan over a patterning device image; concurrently, the substrate table WT is simultaneously moved in the same or opposite direction at a speed V=Mv, in which M is the magnification of the lens PS (typically, M=¼ or ⅕). In this manner, a relatively large target portion C can be exposed, without having to compromise on resolution.

FIG. **12** schematically depicts another exemplary lithographic projection apparatus **1000** whose illumination source could be optimized utilizing the methods described herein.

The lithographic projection apparatus **1000** includes:

a source collector module SO

an illumination system (illuminator) IL configured to condition a radiation beam B (e.g. EUV radiation).

a support structure (e.g. a mask table) MT constructed to support a patterning device (e.g. a mask or a reticle) MA and connected to a first positioner PM configured to accurately position the patterning device;

a substrate table (e.g. a wafer table) WT constructed to hold a substrate (e.g. a resist coated wafer) W and connected to a second positioner PW configured to accurately position the substrate; and

a projection system (e.g. a reflective projection system) PS configured to project a pattern imparted to the radiation beam B by patterning device MA onto a target portion C (e.g. comprising one or more dies) of the substrate W.

As here depicted, the apparatus **1000** is of a reflective type (e.g. employing a reflective mask). It is to be noted that because most materials are absorptive within the EUV wavelength range, the mask may have multilayer reflectors comprising, for example, a multi-stack of Molybdenum and Silicon. In one example, the multi-stack reflector has a 40 layer pairs of Molybdenum and Silicon where the thickness of each layer is a quarter wavelength. Even smaller wavelengths may be produced with X-ray lithography. Since most material is absorptive at EUV and x-ray wavelengths, a thin piece of patterned absorbing material on the patterning device topography (e.g., a TaN absorber on top of the multi-layer reflector) defines where features would print (positive resist) or not print (negative resist).

Referring to FIG. **12**, the illuminator IL receives an extreme ultra violet radiation beam from the source collector module SO. Methods to produce EUV radiation include, but are not necessarily limited to, converting a material into a plasma state that has at least one element, e.g., xenon, lithium or tin, with one or more emission lines in the EUV range. In one such method, often termed laser produced plasma ("LPP") the plasma can be produced by irradiating a fuel, such as a droplet, stream or cluster of material having the line-emitting element, with a laser beam. The source collector module SO may be part of an EUV radiation system including a laser, not shown in FIG. **12**, for providing the laser beam exciting the fuel. The resulting plasma emits output radiation, e.g., EUV radiation, which is collected using a radiation collector, disposed in the source collector module. The laser and the source collector module may be separate entities, for example when a CO_2 laser is used to provide the laser beam for fuel excitation.

In such cases, the laser is not considered to form part of the lithographic apparatus and the radiation beam is passed from the laser to the source collector module with the aid of a beam delivery system comprising, for example, suitable directing mirrors and/or a beam expander. In other cases the source may be an integral part of the source collector module, for example when the source is a discharge produced plasma EUV generator, often termed as a DPP source.

The illuminator IL may comprise an adjuster for adjusting the angular intensity distribution of the radiation beam. Generally, at least the outer and/or inner radial extent (commonly referred to as σ-outer and σ-inner, respectively) of the intensity distribution in a pupil plane of the illuminator can be adjusted. In addition, the illuminator IL may comprise various other components, such as facetted field and pupil mirror devices. The illuminator may be used to condition the radiation beam, to have a desired uniformity and intensity distribution in its cross section.

The radiation beam B is incident on the patterning device (e.g., mask) MA, which is held on the support structure (e.g., mask table) MT, and is patterned by the patterning device. After being reflected from the patterning device (e.g. mask) MA, the radiation beam B passes through the projection system PS, which focuses the beam onto a target portion C of the substrate W. With the aid of the second positioner PW and position sensor PS**2** (e.g. an interferometric device, linear encoder or capacitive sensor), the substrate table WT can be moved accurately, e.g. so as to position different target portions C in the path of the radiation beam B. Similarly, the first positioner PM and another position sensor PS**1** can be used to accurately position the patterning device (e.g. mask) MA with respect to the path of the radiation beam B. Patterning device (e.g. mask) MA and substrate W may be aligned using patterning device alignment marks M**1**, M**2** and substrate alignment marks P**1**, P**2**.

The depicted apparatus **1000** could be used in at least one of the following modes:

1. In step mode, the support structure (e.g. mask table) MT and the substrate table WT are kept essentially stationary, while an entire pattern imparted to the radiation beam is projected onto a target portion C at one time (i.e. a single static exposure). The substrate table WT is then shifted in the X and/or Y direction so that a different target portion C can be exposed.

2. In scan mode, the support structure (e.g. mask table) MT and the substrate table WT are scanned synchronously while a pattern imparted to the radiation beam is projected onto a target portion C (i.e. a single dynamic exposure). The velocity and direction of the substrate table WT relative to the support structure (e.g. mask table) MT may be determined by the (de-)magnification and image reversal characteristics of the projection system PS.

3. In another mode, the support structure (e.g. mask table) MT is kept essentially stationary holding a programmable patterning device, and the substrate table WT is moved or scanned while a pattern imparted to the radiation beam is projected onto a target portion C. In this mode, generally a pulsed radiation source is employed and the programmable patterning device is updated as required after each movement of the substrate table WT or in between successive radiation pulses during a scan. This mode of operation can be readily applied to maskless lithography that utilizes programmable patterning device, such as a programmable mirror array of a type as referred to above.

FIG. **13** shows the apparatus **1000** in more detail, including the source collector module SO, the illumination system IL, and the projection system PS. The source collector module

SO is constructed and arranged such that a vacuum environment can be maintained in an enclosing structure **220** of the source collector module SO. An EUV radiation emitting plasma **210** may be formed by a discharge produced plasma source. EUV radiation may be produced by a gas or vapor, for example Xe gas, Li vapor or Sn vapor in which the very hot plasma **210** is created to emit radiation in the EUV range of the electromagnetic spectrum. The very hot plasma **210** is created by, for example, an electrical discharge causing an at least partially ionized plasma. Partial pressures of, for example, 10 Pa of Xe, Li, Sn vapor or any other suitable gas or vapor may be required for efficient generation of the radiation. In an embodiment, a plasma of excited tin (Sn) is provided to produce EUV radiation.

The radiation emitted by the hot plasma **210** is passed from a source chamber **211** into a collector chamber **212** via an optional gas barrier or contaminant trap **230** (in some cases also referred to as contaminant barrier or foil trap) which is positioned in or behind an opening in source chamber **211**. The contaminant trap **230** may include a channel structure. Contamination trap **230** may also include a gas barrier or a combination of a gas barrier and a channel structure. The contaminant trap or contaminant barrier **230** further indicated herein at least includes a channel structure, as known in the art.

The collector chamber **211** may include a radiation collector CO which may be a so-called grazing incidence collector. Radiation collector CO has an upstream radiation collector side **251** and a downstream radiation collector side **252**. Radiation that traverses collector CO can be reflected off a grating spectral filter **240** to be focused in a virtual source point IF along the optical axis indicated by the dot-dashed line 'O'. The virtual source point IF is commonly referred to as the intermediate focus, and the source collector module is arranged such that the intermediate focus IF is located at or near an opening **221** in the enclosing structure **220**. The virtual source point IF is an image of the radiation emitting plasma **210**.

Subsequently the radiation traverses the illumination system IL, which may include a facetted field mirror device **22** and a facetted pupil mirror device **24** arranged to provide a desired angular distribution of the radiation beam **21**, at the patterning device MA, as well as a desired uniformity of radiation intensity at the patterning device MA. Upon reflection of the beam of radiation **21** at the patterning device MA, held by the support structure MT, a patterned beam **26** is formed and the patterned beam **26** is imaged by the projection system PS via reflective elements **28**, **30** onto a substrate W held by the substrate table WT.

More elements than shown may generally be present in illumination optics unit IL and projection system PS. The grating spectral filter **240** may optionally be present, depending upon the type of lithographic apparatus. Further, there may be more mirrors present than those shown in the figures, for example there may be 1-6 additional reflective elements present in the projection system PS than shown in FIG. **13**.

Collector optic CO, as illustrated in FIG. **13**, is depicted as a nested collector with grazing incidence reflectors **253**, **254** and **255**, just as an example of a collector (or collector mirror). The grazing incidence reflectors **253**, **254** and **255** are disposed axially symmetric around the optical axis O and a collector optic CO of this type is preferably used in combination with a discharge produced plasma source, often called a DPP source.

Alternatively, the source collector module SO may be part of an LPP radiation system as shown in FIG. **14**. A laser LA is arranged to deposit laser energy into a fuel, such as xenon (Xe), tin (Sn) or lithium (Li), creating the highly ionized plasma **210** with electron temperatures of several 10's of eV. The energetic radiation generated during de-excitation and recombination of these ions is emitted from the plasma, collected by a near normal incidence collector optic CO and focused onto the opening **221** in the enclosing structure **220**.

The concepts disclosed herein may simulate or mathematically model any generic imaging system for imaging sub wavelength features, and may be especially useful with emerging imaging technologies capable of producing wavelengths of an increasingly smaller size. Emerging technologies already in use include EUV (extreme ultra violet) lithography that is capable of producing a 193 nm wavelength with the use of an ArF laser, and even a 157 nm wavelength with the use of a Fluorine laser. Moreover, EUV lithography is capable of producing wavelengths within a range of 20-5 nm by using a synchrotron or by hitting a material (either solid or a plasma) with high energy electrons in order to produce photons within this range.

While the concepts disclosed herein may be used for imaging on a substrate such as a silicon wafer, it shall be understood that the disclosed concepts may be used with any type of lithographic imaging systems, e.g., those used for imaging on substrates other than silicon wafers.

The invention may further be described using the following clauses:

1. A computer-implemented method for improving a lithographic process for imaging a portion of a design layout onto a substrate using a lithographic projection apparatus, the method comprising:

defining a multi-variable cost function, the multi-variable cost function being a function of a stochastic effect of the lithographic process, the stochastic effect being a function of a plurality of design variables that are characteristics of the lithographic process; and

reconfiguring one or more of the characteristics of the lithographic process by adjusting one or more of the design variables until a certain termination condition is satisfied.

2. The method of clause 1, wherein the portion of the design layout comprises one or more selected from the following: an entire design layout, a clip, a section of a design layout that is known to have one or more critical features, a section of the design layout where a hot spot or a warm spot has been identified, and a section of the design layout where one or more critical features have been identified.

3. The method of clause 1 or clause 2, wherein the termination condition includes one or more selected from the following: minimization of the cost function; maximization of the cost function; reaching a certain number of iterations; reaching a value of the cost function equal to or beyond a certain threshold value; reaching a certain computation time; reaching a value of the cost function within an acceptable error limit; and/or minimizing an exposure time in the lithographic process.

4. The method of any of clauses 1 to 3, wherein one or more of the design variables are characteristics of an illumination source for the lithographic apparatus, and/or one or more of the design variables are characteristics of the design layout, and/or one or more of the design variables are characteristics of projection optics of the lithographic apparatus, and/or one or more of the design variables are characteristics of a resist of the substrate.

5. The method of any of clauses 1 to 4, wherein the iterative reconfiguration comprises constraints dictating a range of at least some of the design variables.

6. The method of clause 5, wherein at least some of the design variables are under constraints representing physical restrictions in a hardware implementation of the lithographic projection apparatus.

7. The method of clause 6, wherein the constraints include one or more selected from: a tuning range, a rule governing patterning device manufacturability, and/or interdependence between the design variables.

8. The method of clause 6, wherein the constraints include a throughput of the lithographic projection apparatus.

9. The method of any of clauses 1 to 8, wherein the cost function is a function of one or more of the following lithographic metrics: edge placement error, critical dimension, resist contour distance, worst defect size, and/or best focus shift.

10. The method of any of clauses 1 to 9, comprising, prior to performing the iterative reconfiguration, selecting a subset of target patterns that characteristically represents features of the portion of the design layout.

11. The method of any of clauses 1 to 10, wherein optimization of various design variables are performed simultaneously until the termination condition is satisfied.

12. The method of any of clauses 1 to 10, wherein optimization of various design variables are performed alternatively, keeping at least one of the design variables fixed while the another design variables is optimized, and

repeating the alternative optimization process until the termination condition is satisfied.

13. The method of any of clauses 1 to 12, comprising iteratively minimizing the cost function by calculating linear fitting coefficients within certain relatively small neighborhoods around a starting point in each iteration.

14. The method of clause 13, wherein the cost function is minimized by a method selected from a group consisting of the Gauss-Newton algorithm, the Levenberg-Marquardt algorithm, the gradient descent algorithm, simulated annealing, and the genetic algorithm.

15. The method of any of clauses 1 to 14, wherein the cost function comprises characteristics of a resist image or an aerial image.

16. The method of any of clauses 1 to 15, wherein the cost function is minimized by solving a quadratic programming problem.

17. The method of any of clauses 1 to 16, wherein the cost function is a function of only the design variables that are characteristics of a projection optics of the lithographic apparatus, while other design variables are assigned values.

18. The method of any of clauses 1 to 16, wherein the cost function represents a probability of finding a hot spot in the portion of the design layout.

19. The method of any of clauses 1 to 18, wherein the stochastic effect comprises line width roughness (LWR), a throughput of the lithographic projection apparatus and/or local CD variation.

20. The method of clause 19, wherein the stochastic effect is simulated using a model of the stochastic effect.

21. The method of any of clauses 1 to 20, wherein the stochastic effect is caused by photon shot noise, photon-generated secondary electrons, photon-generated acid in a resist of the substrate, distribution of photon-activatable or electron-activatable particles in a resist of the substrate, density of photon-activatable or electron-activatable particles in a resist of the substrate, or a combination thereof.

22. A computer-implemented method for increasing a throughput of a lithographic process for imaging a portion of a design layout onto a substrate using a lithographic projection apparatus, the method comprising:

defining a multi-variable cost function, the multi-variable cost function being a function of a stochastic effect of the lithographic process, and being a function of an exposure time of the substrate in the lithographic projection apparatus, the stochastic effect being a function of a plurality of design variables that are characteristics of the lithographic process; and

reconfiguring one or more of the characteristics of the lithographic process by adjusting one or more of the design variables until a certain termination condition is satisfied.

23. The method of clause 22, wherein the termination condition is that the exposure time is minimized.

24. The method of any of clauses 1 to 23, wherein the multi-variable cost function is a function of the local CD variation, a throughput of the lithographic projection apparatus, and a stochastic effect of the lithographic process.

25. The method of any of clauses 1 to 23, wherein the multi-variable cost function is a function of an edge placement error, a throughput of the lithographic projection apparatus, and a stochastic effect of the lithographic process.

26. A computer program product comprising a computer readable medium having instructions recorded thereon, the instructions when executed by a computer implementing the method of any of the above clauses. The descriptions above are intended to be illustrative, not limiting. Thus, it will be apparent to one skilled in the art that modifications may be made as described without departing from the scope of the claims set out below.

What is claimed is:

1. A computer-implemented method for improving a lithographic process for imaging a portion of a design layout onto a substrate using a lithographic projection apparatus, the method comprising:

determining a stochastic effect function of the lithographic process that produces as an output a value of a stochastic effect as a function of a plurality of design variables associated with the lithographic process that are inputs to the function and which cause quantifiable changes in the stochastic effect value, wherein the plurality of design variables include at least an adjustable parameter of projection optics of the lithographic process;

defining a multi-variable cost function using the stochastic effect function of the lithographic process such that the multi-variable cost function includes the adjustable parameter of projection optics that causes the quantifiable changes in the stochastic effect value for a desired substrate throughput of the lithographic projection apparatus; and

reconfiguring, by the computer, one or more characteristics of the lithographic process by adjusting one or more of the design variables until a certain termination condition of the cost function is satisfied, thereby achieving the desired substrate throughput.

2. The method of claim **1**, wherein the stochastic effect is simulated using a model of the stochastic effect.

3. The method of claim **2**, wherein the model of the stochastic effect combines line width roughness (LWR) with critical dimension uniformity (CDU).

4. The method of claim **1**, further comprising selecting the portion of the design layout from one or more of the following: an entire design layout, a clip, a section of a design layout that is known to have one or more critical features, a section of the design layout where a hot spot or a warm spot has been identified, and a section of the design layout where one or more critical features have been identified.

5. The method of claim **1**, wherein the termination condition includes one or more selected from the following: minimization of the cost function; maximization of the cost function; reaching a certain number of iterations; reaching a value of the cost function equal to or beyond a certain threshold value; reaching a certain computation time; reaching a value of the cost function within an acceptable error limit; and/or minimizing an exposure time in the lithographic process.

6. The method of claim **1**, wherein one or more of the design variables are characteristics of an illumination source for the lithographic apparatus, and/or one or more of the design variables are characteristics of the design layout, and/or one or more of the design variables are characteristics of projection optics of the lithographic apparatus, and/or one or more of the design variables are characteristics of a resist of the substrate.

7. The method of claim **1**, wherein the reconfiguration comprises constraints dictating a range of at least some of the design variables.

8. The method of claim **7**, wherein at least some of the design variables are under constraints representing physical restrictions in a hardware implementation of the lithographic projection apparatus.

9. The method of claim **8**, wherein the constraints include one or more selected from: a tuning range, a rule governing patterning device manufacturability, and/or interdependence between the design variables.

10. The method of claim **8**, wherein the constraints are determined by the desired substrate throughput of the lithographic projection apparatus.

11. The method of claim **1**, wherein the cost function is a function of one or more of the following lithographic metrics: edge placement error, critical dimension, resist contour distance, worst defect size, and/or best focus shift.

12. The method of claim **1**, wherein the cost function comprises characteristics of a resist image or an aerial image.

13. The method of claim **1**, wherein the cost function is minimized by solving a quadratic programming problem.

14. The method of claim **1**, wherein the cost function represents a probability of finding a hot spot in the portion of the design layout.

15. The method of claim **1**, wherein the multi-variable cost function is a function of an edge placement error, the desired substrate throughput of the lithographic projection apparatus, a dose of a lithographic projection apparatus, and a stochastic effect of the lithographic process.

16. A computer program product comprising a non-transitory computer readable medium having instructions recorded thereon, the instructions when executed by a computer implementing the method of claim **1**.

17. The method of claim **1**, wherein the adjustable parameter of the projection optics represents adjustments to a wavefront manipulator of the lithographic process.

18. The method of claim **1**, wherein the plurality of design variables that are inputs to the function and which cause quantifiable changes to the stochastic effect value further include at least a parameter of the design layout.

19. The method of claim **1**, wherein the stochastic effect is attributed to one or more of the following factors: photon shot noise, photon-generated secondary electrons, photon-generated acids in a resist of the substrate, a distribution of photon-activable or electron-activable particles in a resist of the substrate, and a density of photon-activable or electron-activable particles in a resist of the substrate.

20. The method of claim **1**, wherein the method further comprises: generating an output file to be stored in the computer, the output file comprising adjusted values of the one or more design variables at the termination condition that result in reduced stochastic effects.

21. The method of claim **1**, wherein the adjusted values of the one or more design variables result in an expanded lithography process window.

22. The method of claim **1**, wherein the lithographic process uses extreme ultra-violet (EUV) wavelength.

23. A computer-implemented method for increasing a substrate throughput of a lithographic process for imaging a portion of a design layout onto a substrate using a lithographic projection apparatus, the method comprising:

determining a stochastic effect function of the lithographic process that produces as an output a value of a stochastic effect as a function of a plurality of design variables associated with the lithographic process that are inputs to the function and which cause quantifiable changes in the stochastic effect value, wherein the plurality of design variables include at least an adjustable parameter of projection optics of the lithographic process;

defining a multi-variable cost function using the stochastic effect function of the lithographic process such that the multi-variable cost function includes the adjustable parameter of projection optics that causes the quantifiable changes in the stochastic effect value for a desired substrate throughput of the lithographic projection apparatus, the cost function further being a function of an exposure time of the substrate in the lithographic projection apparatus; and

reconfiguring, by the computer, one or more characteristics of the lithographic process by adjusting one or more of the design variables until a certain termination condition of the cost function is satisfied, thereby achieving the desired substrate throughput.

24. The method of claim **23**, wherein the termination condition is that the exposure time is minimized.

25. The method of claim **23**, wherein the stochastic effect is attributed to one or more of the following factors: photon shot noise, photon-generated secondary electrons, photon-generated acids in a resist of the substrate, a distribution of photon-activable or electron-activable particles in a resist of the substrate, and a density of photon-activable or electron-activable particles in a resist of the substrate.

26. The method of claim **23**, wherein the method further comprises: generating an output file to be stored in the computer, the output file comprising adjusted values of the one or more design variables at the termination condition that result in reduced stochastic effects.

27. The method of claim **23**, wherein the lithographic process uses extreme ultra-violet (EUV) wavelength.

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